BL0906

Six-phase AC/DC power metering chip

Data Sheet

V1.10

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1.Product Description

BL0906It is a multi-channel calibration-free energy metering chip with built-in clock, which can realize AC/DC energy metering of up to six phases.5GMacro base station DC detection module, data center intelligencePDU, and other multi-channel electricity metering and fault detection fields, with high cost performance.

BL0906Integrated7Road high precisionSigma-Delta ADC, can simultaneously measure6Road current,1Road voltage.

BL0906It can measure current, voltage RMS, active power, active electric energy and other parameters, and can output fast current RMS (for leakage monitoring, overcurrent protection and other fault detection), as well as temperature detection, waveform output and other functions. UARTor high speedSPIThe interface outputs data that can fully meet5GMacrocells, data center intelligencePDU, and other big data collection needs.

BL0906For the input waveform, you can also select different filters to obtain the full wave, fundamental wave or DC effective value and power.

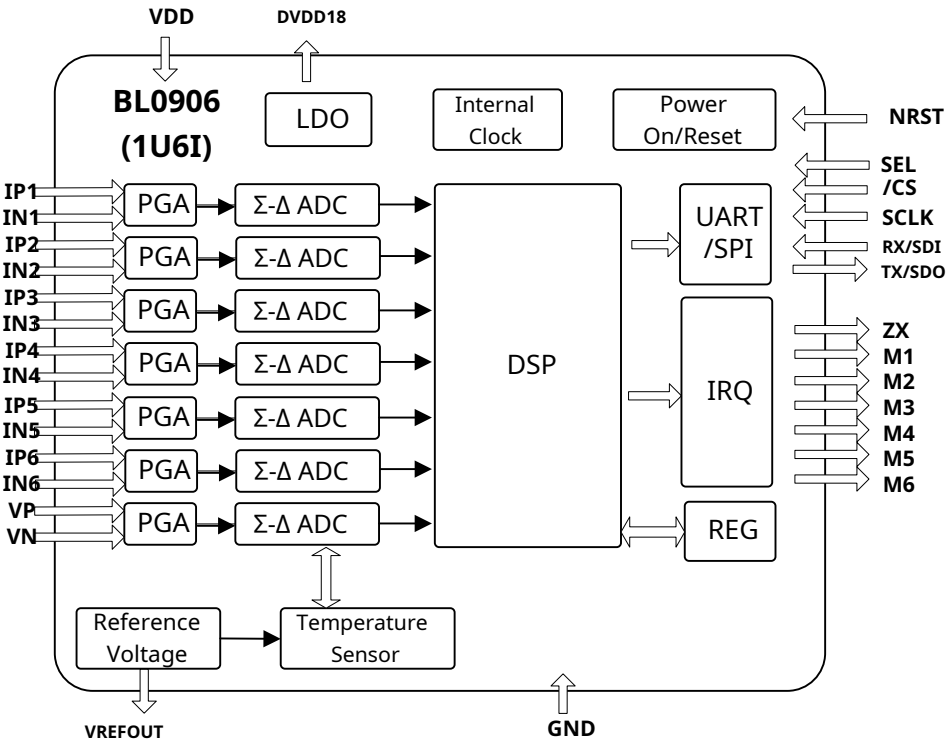
BL0906Factory channel measurement gain deviation is calibrated to <1%When the whole machine is not calibrated and a high-precision sampling resistor is used externally, the measurement error of the whole machine is less than2%If you need to meet high-precision measurement requirements (machine error <0.3%), external calibration is required.

2.Basic Features

2.1Main Features

- Measurement channels include6Current channels,1Voltage channels
- High accuracy, over the input dynamic range (5000:1), the nonlinear measurement error of active energy is less than0.1%
- RMS values of voltage and current, measurement dynamic range (2500:1), the effective value error is less than0.1%
- For the input waveform, you can select different filters to obtain the full wave, fundamental wave or DC effective value and power.
- Optional DC signal measurement, input dynamic range2000:1, nonlinear error of electric energy measurement <±1%,
- The gain error of the batch is less than1%
- Built-in waveform registers for waveform analysis
- Leakage monitoring function, can measure1mAAbove leakage, shortest response time10mS, leakage monitoring threshold and response time can be set
- Each channel has an overcurrent output indication, and the overcurrent threshold and response time can be set
- Built-in temperature sensor, measuring range -40Degree~85Degree, measurement accuracy ±3To meet the needs of product over-temperature monitoring, high current node preset temperature quotation, room temperature measurement, etc.
- Load form can be analyzed
- Built-in active power, energy, current\voltage effective value and angle registers
- UART/SPIinterface
- Anti-creep design ensures noise removal when there is no current
- Power failure detection, below2.7VWhen the chip is reset
- Built-in reference voltage source
- Built-in oscillation circuit, clock approx.8MHz
- Single working power supply3.3V, low power consumption30mW(Typical value)
- LQFP32Encapsulation
- Note: The error within the input dynamic range refers to the accuracy after the whole machine is calibrated.

2.2System Block Diagram



2.3Pin arrangement (LQFP32)

Sorting	Pin Function	I/O	Pin Description
1	IP4	I	#4_Current channel positive input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
2	VREF	I/O	Reference voltage input and output terminal, external0.1uFFilter capacitor
3	IN5	I	#5_Current channel negative input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
4	IP5	I	#5_Current channel positive input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
5	IN6	I	#6_Current channel negative input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
6	IP6	I	#6_Current channel positive input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
7	VN	I	Voltage channel negative input, maximum differential voltage ±0.7V
8	VP	I	Voltage channel positive input, maximum differential voltage ±0.7V

9	/RST	I	Reset pin, low level is effective
10	GND	I	land
11	/CS	I	SPIChip select signal pin
12	TX/SDO	O	SPI/UARTCommunication pin, send
13	RX/SDI	I	SPI/UARTCommunication pin, receive
14	SCLK	I	SPICommunication clock
15	ZX	O	Voltage fundamental wave zero-crossing output
16	VPP	I	Reserved, can be left floating
17	M1	O	aisle1Overcurrent output/active power calibration pulse output
18	M2	O	aisle2Overcurrent output/reactive power meter calibration pulse output
19	M3	O	aisle3Overcurrent output
20	M4	O	aisle4Overcurrent output
twenty one	M5	O	aisle5Overcurrent output
twenty two	M6	O	aisle6Overcurrent output
twenty three	DVDD18	I	1.8VVoltage, external0.1uFFilter capacitor
twenty four	SEL	I	Sel=0Time to chooseUart(default),Sel=1Time to chooseSPI.
25	VDD	I	Power Input
26	IN1	I	#1_Current channel negative input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
27	IP1	I	#1_Current channel positive input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
28	IN2	I	#2_Current channel negative input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
29	IP2	I	#2_Current channel positive input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
30	IN3	I	#3_Current channel negative input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
31	IP3	I	#3_Current channel positive input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.
32	IN4	I	#4_Current channel negative input. Analog input, gainx1~x16Adjustable. Each pair of pins The maximum differential voltage is±0.7V.

2.4Performance Indicators

2.4.1Electrical parameter performance index

(VDD = 3.3V, GND = 0V, 25 ℃, Energy accuracy error measure via CF output)

Parameter	Symbol	Test Condition	Measure Pin	Min	Type	Max	Unit
Active power measurement error Difference	WATTERR	5000:1 input DR			0.1		%
Reactive power measurement error Difference	VARERR	5000:1 input DR			0.1		%
The phase angle between channels causes Measurement error (PF=0.8Capacitive) (PF=0.5Sensual	 PF08CERR PF05LERR	 Phase Advance37° Phase lag60°			 0.1 0.1		 % %
ACPower Supply Rejection (Output frequency amplitude change) DCPower Supply Rejection (Output frequency amplitude change)	ACPSRR DCPSRR	Current channel input pin IP\IN@100mV,Voltage Channel input pin VP\VN=100mV			0.01 0.1		% %
Voltage RMS measurement Accuracy, relative error	VRMSERR	2500:1 input DR			0.1		%
Current RMS measurement Accuracy, relative error	IRMSERR	2500:1 input DR			0.1		%
Analog Input Input level (peak) Input Impedance bandwidth(-3dB) Gain Error Phase gain matching error Difference		 Differential input external1.2Reference voltage external1.2Reference voltage			 370 14 0.5 0.3	 700	 mV kΩ kHz % %
Internal voltage reference Benchmark Deviation Temperature coefficient	Vref VrefERR TempCoef				1.097 5 20		V mV ppm/℃

Logic Input /RST, RX/SDI, SCLK、/CS Input high level Input low level		DVDD=3.3V±2.5% DVDD=3.3V±2.5%		2.6		0.8	V V
Logic Output TX/SDO,M1-M10, CF_WATT, CF_VAR Output high level Output low level		DVDD=3.3V±2.5% DVDD=3.3V±2.5%		2.6		1	V V
power supply VDD, DVDD18 IDD	VVDD VDVDD18 IVDD	DVDD18=1.8V VDD=3.3		3 1.62	3.3 1.8 9	3.6 2 16	V V mA

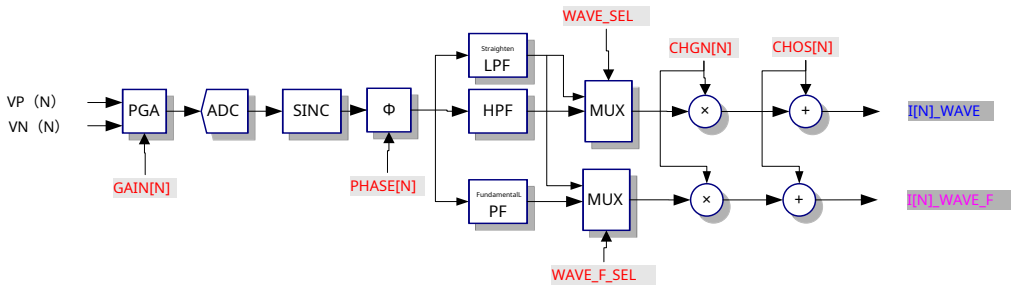
2.4.2Limit range

(T = 25℃)

project	symbol	extremum	unit
Supply voltageVDD	VDD	-0.3 ~ +4	V
Supply voltageDVDD18	DVDD18	-0.3 ~ +2.5	V
Analog input voltage (relative toGND)	IN1,IP1,IN2,IP2,IN3,IN3, IN4,IP4, IN5,IP5,IN6,IP6, VP,VN	-1 ~ +VDD	V
Analog output voltage (relative toGND)	Vref	- 0.3 ~ +VDD	V
Digital input voltage (relative toGND)	SEL、/RST,RX/SDI,SCLK、/CS	- 0.3 ~ VDD+0.3	V
Digital output voltage (relative toGND)	M1,M2,M3,M4,M5,M6, TX/SDO,IRQ	- 0.3 ~ VDD+0.3	V
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstr	-55 ~ +150	℃
Power consumption (LQFP32)	P	200	mW

3.How it works

3.1Current and voltage waveform generation principle



Total7High precision of the same structureADC, using double-ended differential signal input:NThe positive and negative voltage signals of the current channel input areVP[N]andVN[N].

7Waveform output, including6The current and1Road voltage.

In the channel (same current and voltage, same circuit structure) , the input signal passes through the analog module amplifier (PGA)and High-precision analog-to-digital conversion (ADC) converts the analog signal into a digital signal. The digital signal is phase compensated and down-sampled by a filter (SINC), optional high-pass filter (HPF) or fundamental wave low-pass filter or DC low-pass filter, and then through gain and offset correction modules, the required current waveform data and voltage waveform data are obtained (I[N]_WAVE, V_WAVE).

7ChannelPGAGain adjustable, channelPGAGain Adjust RegisterGAIN1andGAIN2The data format is as follows:4Bit controls one channel,0000=1;0001=2;0010=8;0011=16） .

address	name	Bit width	default value	describe
60	GAIN1	twenty four	0x000000	aislePGAGain Adjust Register [3:0]: voltage channel; [11:8]: Current1aisle [15:12]: Current2aisle;[19:16]: Current3aisle [23:20]: Current4aisle
61	GAIN2	20	0x00000	aislePGAGain Adjust Register [11:8]: Current5aisle;[15:12]: Current6aisle

3.1.1Channel offset correction

Include7indivual16Channel offset calibration registerCHOS[N], the default value is0x0000.

They2The data in the form of two's complement is used to eliminate the deviation caused by the analog-to-digital conversion of the current channel and the voltage channel. The deviation here may be caused by the input and the analog-to-digital conversion circuit itself.offsetDeviation correction can make the waveform in no-load condition offsetfor0.

7The channel offset of the channel is adjustable, the channel offset adjustment registerCHOS[N]The correction formula is as follows:

address	name	Bit width	default value	describe
AC	CHOS[1]	16	0x0000	Current1Channel offset adjustment register, two's complement
AD	CHOS[2]	16	0x0000	Current2Channel offset adjustment register, two's complement
AE	CHOS[3]	16	0x0000	Current3Channel offset adjustment register, two's complement
AF	CHOS[4]	16	0x0000	Current4Channel offset adjustment register, two's complement
B2	CHOS[5]	16	0x0000	Current5Channel offset adjustment register, two's complement
B3	CHOS[6]	16	0x0000	Current6Channel offset adjustment register, two's complement
B5	CHOS[V]	16	0x0000	Voltage channel offset adjustment register, two's complement

Bias adjustment correction formula:

$$WAVE[N] = WAVE0[N] + CHOS[N]$$

inWAVE0[N]For theNThe measured value of the channel,CHOS[N]is the calibration value,WAVE[N]Output after calibration value.

3.1.2Channel gain correction

Include7indivual16Channel Gain Calibration RegisterCHGN[N], the default value is0x0000.

They2The gain error caused by the analog-to-digital conversion of the current channel and voltage channel can be adjusted by using the data in the form of the two's complement. The error here may be caused by the input and the analog-to-digital conversion circuit itself. Gain correction can make the positive and negative50%Adjust within range.

7The channel gain of the channel is adjustable, the channel gain adjustment registerCHGN[N]The correction formula is as follows:

address	name	Bit width	default value	describe
A1	CHGN[1]	16	0x0000	Current1Channel gain adjustment register, two's complement
A2	CHGN[2]	16	0x0000	Current2Channel gain adjustment register, two's complement
A3	CHGN[3]	16	0x0000	Current3Channel gain adjustment register, two's complement
A4	CHGN[4]	16	0x0000	Current4Channel gain adjustment register, two's complement
A7	CHGN[5]	16	0x0000	Current5Channel gain adjustment register, two's complement
A8	CHGN[6]	16	0x0000	Current6Channel gain adjustment register, two's complement
AA	CHGN[V]	16	0x0000	Voltage channel gain adjustment register, two's complement

Channel gain correction formula:

$$WAVE[N] = WAVE0[N] * (1 + \frac{CHGN[N]}{2^{16}})$$

inWAVE0[N]For theNThe measured value of the channel,CHGN[N]is the gain calibration value,WAVE[N]For calibration output value.

3.1.3Current and voltage waveform output

Can collect current load current and voltage waveform data, sample current and voltage to15kspsUpdate rate, sampling per cycle300Each sampling data is24bitSigned numbers are stored in waveform registers (I[N]_WAVE, V_WAVE). The waveform values of multiple channels can be read continuously.

You can select channel full wave, AC full wave, fundamental wave and DC waveform respectively, and finally get7Channel waveform (normal current and fast current optional).

address	name	Bit width	default value	describe
2	I[1]_WAVE	twenty four	0x000000	Current1Channel waveform register
3	I[2]_WAVE	twenty four	0x000000	Current2Channel waveform register
4	I[3]_WAVE	twenty four	0x000000	Current3Channel waveform register
5	I[4]_WAVE	twenty four	0x000000	Current4Channel waveform register
8	I[5]_WAVE	twenty four	0x000000	Current5Channel waveform register
9	I[6]_WAVE	twenty four	0x000000	Current6Channel waveform register
B	V_WAVE	twenty four	0x000000	aisle11Waveform register

The current waveform output selection can be set through the user mode registerMODE1[23]Set up. The voltage waveform output is a normal waveform (the waveform for effective value calculation).

0x96	MODE1	Working Mode Register	
No.	name	default value	description
[twenty three]	WAVE_REG_SEL	1'b0	CurrentWAVEWaveform register output selection: default0 Select the waveform of the normal current channel,1Select Fast Pass Waveform output of the channel

Normal waveforms (waveforms for effective value calculation) are divided into full wave, AC full wave, fundamental wave and DC.HPFOutput full-wave waveform.HPFIn AC measurement mode, it outputs AC full-wave waveform.LPFIn fundamental wave measurement mode, output fundamental wave waveform.LPFIn DC measurement mode, it outputs DC waveform. MODE2To set up, each channel can be set up separately.

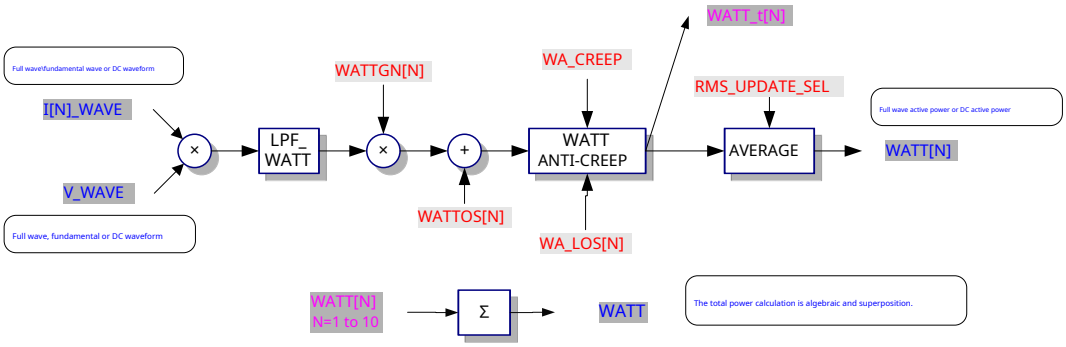
0x97	MODE2	Working Mode Register	
No.	name	default value	description

[21:0]	WAVE_RMS_SEL	11{2'b00}	Effective value waveform selection: 00-AC full wave,10-DC,01-Fundamental wave,11-Full Wave [3:2]: Current1aisle;[5:4]: Current2aisle; [7:6]: Current3aisle;[9:8]: Current4aisle; [15:14]: Current5aisle;[17:16]: Current6aisle; [21:20]: Voltage channel

The waveform of the fast channel (the waveform for fast effective value calculation) is divided into full wave and AC full wave.HPFOutput full-wave waveform.HPFIn AC measurement mode, it outputs AC full-wave waveform. MODE1[22]to set it up.

0x96	MODE1	Working Mode Register	
No.	name	default value	description
[twenty two]	L_F_SEL	1'b0	Fast channel selects whether to pass Qualcomm, the default is0-No Qualcomm,1-Choose Qualcomm

3.2Active power calculation principle



The current and voltage waveforms are digitally multiplied, and then sequentially processed through low-pass filtering, gain and offset calibration, anti-creep judgment and averaging to obtain the power signal.

3.2.1Active power waveform selection

The waveform for power calculation can be obtained through user mode registersMODE1Note: When choosing to calculate DC power, both current and voltage should choose DC waveform for power calculation.

0x96	MODE1	Working Mode Register	
No.	name	default value	description
[10:0]	WAVE_ SEL	11{1'b0}	WATTFull wave waveform selection,0-AC full wave,1-DC [1]: Current1aisle;[2]: Current2aisle;

			[3]: Current3aisle;[4]: Current4aisle; [7]: Current5aisle;[8]: Current6aisle; [10]: Voltage channel

3.2.2Active power output

You can select the channel AC full wave and fundamental wave to obtain6Power signalWATT[N]The active power register istwenty four Bit signed number, two's complement.Bit[23]It is the sign bit, indicating positive work/negative work.

address	name	Bit width	default value	describe
twenty three	WATT[1]	twenty four	0x000000	aisle1Active Power Register
twenty four	WATT[2]	twenty four	0x000000	aisle2Active Power Register
25	WATT[3]	twenty four	0x000000	aisle3Active Power Register
26	WATT[4]	twenty four	0x000000	aisle4Active Power Register
29	WATT[5]	twenty four	0x000000	aisle5Active Power Register
2A	WATT[6]	twenty four	0x000000	aisle6Active Power Register
2C	WATT	twenty four	0x000000	Total active power register

Active power register calculation formula for each channel (typical value):

$$\text{WATT[x]Register value} = \frac{40.4125 * I_N(A) * Gain\_I * V(V) * Gain\_V * Cos(\varnothing)}{Vref^2}$$

in,$I_N(A)$,V(V)is the effective value of the channel pin input voltage (mV),Vrefis the built-in reference voltage, the typical value is1.097V. Value40.4125are typical coefficients.Gain_Iis the current channel gain multiple,Gain_Vis the voltage channel gain multiple.

The active power can be accumulated byMODE3[8]The register is used to set the active power sum obtained by absolute value addition or algebraic sum addition.

0x98	MODE3	Working Mode Register	
No.	name	default value	description
[8]	add_sel	1'b0	WattThe sum of the sum of the phases is:0-Absolute value addition;1-Algebra and addition.

3.2.3Active power calibration

Included6indivual16Active Power Bias Correction RegisterWATTOS[N]and6indivual16Active Power Gain Correction RegisterWATTGN[N], the default value is0x0000.

WATTOSUsed to eliminate DC deviation in active power calculation.WATTGNUsed to eliminate gain deviation in active power calculation. The deviation may be caused byPCBThe crosstalk between the two channels generated by the board and the integrated circuit itself may also beADCGain deviation of the channel itself.

Deviation correction can make the value in the active power register close to0.

address	name	Bit width	default value	describe
B7	WATTGN[1]	16	0x0000	aisle1Active power gain adjustment register, two's complement
B8	WATTGN[2]	16	0x0000	aisle2Active power gain adjustment register, two's complement
B9	WATTGN[3]	16	0x0000	aisle3Active power gain adjustment register, two's complement
BA	WATTGN[4]	16	0x0000	aisle4Active power gain adjustment register, two's complement
BD	WATTGN[5]	16	0x0000	aisle5Active power gain adjustment register, two's complement
BE	WATTGN[6]	16	0x0000	aisle6Active power gain adjustment register, two's complement
C1	WATTOS[1]	16	0x0000	aisle1Active power bias adjustment register, two's complement
C2	WATTOS[2]	16	0x0000	aisle2Active power bias adjustment register, two's complement
C3	WATTOS[3]	16	0x0000	aisle3Active power bias adjustment register, two's complement
C4	WATTOS[4]	16	0x0000	aisle4Active power bias adjustment register, two's complement
C7	WATTOS[5]	16	0x0000	aisle5Active power bias adjustment register, two's complement
C8	WATTOS[6]	16	0x0000	aisle6Active power bias adjustment register, two's complement

Correction result of active power:

$$WATT[N] = WATT0[N] * (1 + \frac{WATTGN[N]}{2^{16}})$$

inWATT[N]It isNActive power after phase correction,WATT0[N]It isNActive work before phase correction Rate.

3.2.4Phase compensation

existADCOutput position, providing a method for digital calibration of small phase errors. It can introduce a small time delay or advance into the signal processing circuit to compensate for small phase errors. Since this compensation must be timely, this method is only applicable to <0.6-Using time-shifting techniques to correct large phase errors can introduce significant phase errors in higher harmonics.

7Channel phase compensation adjustable, phase calibration registerPHASE[N]The data format is as follows (each8bit to calibrate one channel, [7]reserve,[6:0]Minimum adjustment delay time250ns,correspond0.0045Spend/1LSB, maximum adjustable ± 0.5715 Spend.):

address	name	Bit width	default value	describe

64	NA/PHASE[1]	16	0x1010	[15:8]:reserve [7:0]: Current1aisle
65	PHASE[2]/PHASE[3]	16	0x1010	[15:8]: Current2aisle [7:0]: Current3aisle
66	PHASE[4]/NA	16	0x1010	[15:8]: Current4aisle [7:0]:reserve
67	NA/PHASE[5]	16	0x1010	[15:8]:reserve [7:0]: Current5aisle
68	PHASE[6]/NA	16	0x1010	[15:8]: Current6aisle [7:0]:reserve
69	PHASE[V]	8	0x10	Voltage Channel

3.2.5Active power anti-creep

Built-in patented power anti-submarine function module to ensure that the power output is0.

Active anti-creep threshold register (WA_CREEP） ,for12bitUnsigned number, default is04CThis value is internally (Internal times2 0) is compared with the absolute value of the input active power signal. When the absolute value of the input active power signal is less than this value, the output active power is set to zero. This allows the value output to the active power register to be equal to 0 even if there is a small noise signal under no-load conditions.0.

address	name	Bit width	default value	describe
88	VAR_CREEP/ WA_CREEP	twenty four	0x04C04C	[11:0]Active anti-creep power threshold register WA_CREEP;[23:12]Reactive power protection threshold MemoryVAR_CREEP.
89	WA_CREEP2	12	0x000	[11:0]Total active power anti-creep threshold register

The power registerWATTValue SettingWA_CREEPThe default anti-submarine value is approximately 20 millionths of full-scale power.

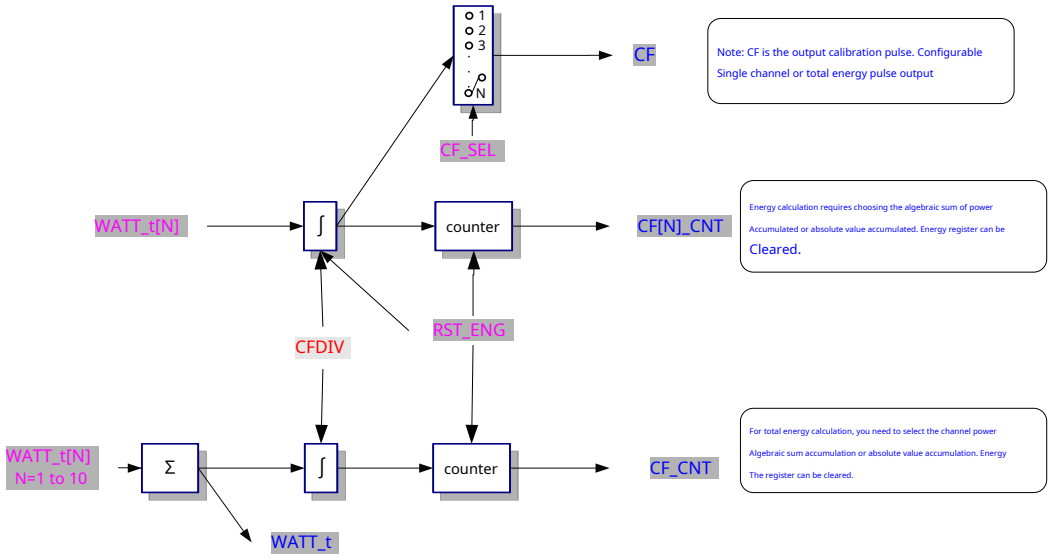
When a channel is in the anti-submarine state, the instantaneous power of the channel below the threshold does not participate in the energy accumulation.

3.2.6Active power small signal compensation

For active power (fundamental wave and full wave) calculation, in order to reduce the noise error in the small signal segment, the small signal compensation register can be used to adjust the nonlinear error of the small signal segment.WA_LOS),for12bit The default is two's complement.000.

address	name	Bit width	default value	describe
82	reserve/ WA_LOS[1]	twenty four	0x000000	[23:12]:reserve [11:0]:aisle1Active power small signal compensation register
83	WA_LOS[2]/ WA_LOS[3]	twenty four	0x000000	[23:12]:aisle2Active power small signal compensation register [11:0]:aisle3Active power small signal compensation register
84	WA_LOS[4]/ reserve	twenty four	0x000000	[23:12]:aisle4Active power small signal compensation register [11:0]:reserve
85	reserve/ WA_LOS[5]	twenty four	0x000000	[23:12]:reserve [11:0]:aisle5Active power small signal compensation register
86	WA_LOS[6]/ reserve	twenty four	0x000000	[23:12]:aisle6Active power small signal compensation register [11:0]:reserve

Active energy measurement principle



supply6The electric energy pulse of the channel is accumulated. The principle is that the active power of each channel can be integrated over a period of time to obtain the active energy during this period, and further convert the energy into the corresponding frequency calibration pulse.CF, high electricity consumption,CFThe frequency is fast and the power consumption is low.CFThe frequency is slow.

3.3Active energy output

rightCFCounting pulses can obtain energy (power consumption) , stored inNPhase energy accumulation register CF[N]_CNTThe total energy is stored in the total energy registerCF_CNT, as shown in the figure below.

address	name	Bit width	default value	describe
30	CF[1]_CNT	twenty four	0x000000	aisle1Active energy pulse count, unsigned
31	CF[2]_CNT	twenty four	0x000000	aisle2Active energy pulse count, unsigned
32	CF[3]_CNT	twenty four	0x000000	aisle3Active energy pulse count, unsigned
33	CF[4]_CNT	twenty four	0x000000	aisle4Active energy pulse count, unsigned
36	CF[5]_CNT	twenty four	0x000000	aisle5Active energy pulse count, unsigned
37	CF[6]_CNT	twenty four	0x000000	aisle6Active energy pulse count, unsigned
39	CF_CNT	twenty four	0x000000	Total active energy pulse count, unsigned

Active energy output selection

Represents the active energyCF_WATTThe pulse can beMODE3To set up and configureM1OutputCF_WATT Pulse, at the same timeM2Output represents the reactive energyCF_VARpulse.

0x98	MODE3	Working Mode Register	
No.	name	default value	description
[9]	cf_enable	1'b0	0-cf disable,default;1-cf enable
[13:10]	CF_SEL	4'b0000	aisleCF_WATTOutput selection: 0000,1110,1111-Default offCF; 0010-aisle1PowerCF;0011-aisle2PowerCF; 0100-aisle3PowerCF;0101-aisle4PowerCF; 1000-aisle5PowerCF;1001-aisle6PowerCF; 1011-Total active powerCF; 1100-Reactive powerCF(channel optional); 1101-Apparent powerCF(channel optional); Other,CF_VARReactive powerCF(Channel optional) unchanged
[15]	cf_add_sel	1'b0	WattandvarEnergy adding method: 0-Absolute value addition;1-Algebraic Sum and Addition (Partitions and Conjunctions)

Set up firstMODE3[9]=1Select ConfigureM1,M2Output separatelyCF_WATTPulse andCF_VARPulse, then setCF_SELThe calibration pulse output of any channel can be selected for calibration.CFThe pulse period is less than180mS Time50%Duty cycle pulse, period is greater than or equal to180mSFixed high level pulse width90mS.

CF_add_selIt can be used to set how the total energy is added, the algebraic sum of each phase or the absolute value.

CFThe pulse counting results are stored inCF[N]_CNTregister, or byM1（CF) pin directly counts the number of pulses.CFThe period is less than180msWhen50%Pulse duty cycle greater than or equal to180ms When the high level fixed pulse width90ms.

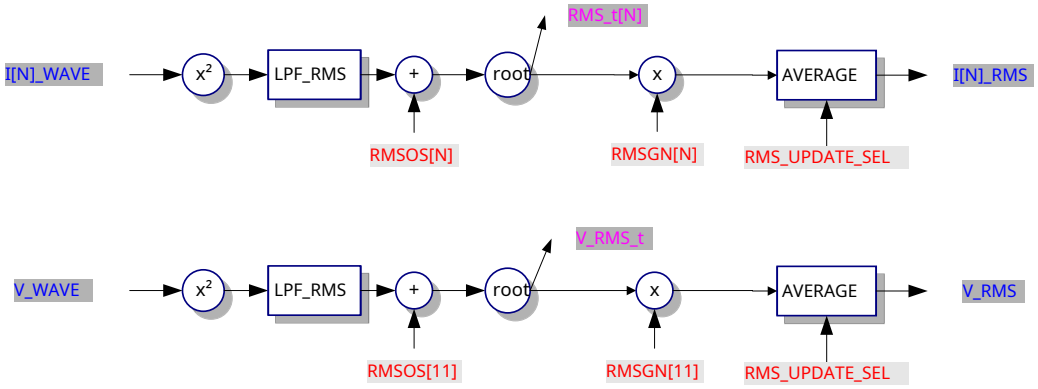
Active energy output ratio

Energy is accumulating and can beCF_DIVThe register sets the speed of energy accumulation, each level2times relationship, total12 For coarse adjustment.

address	name	Bit width	default value	describe
CE	CFDIV	12	0x010	CFScaling register

3.4Principle of current and voltage effective value calculation

The effective value principle of the channel is as shown below:



The original waveform of each channel is passed through the square circuit (X2) , effective value low pass filter (LPF_RMS), Open root Circuit (ROOT), get the instantaneous value of the effective valueRMS_t, and then average to get the average value of each channel I[N]RMS andV_RMS.

3.4.1Effective value output

The effective value calculation result is input to7A valid value register, which istwenty fourUnsigned bit number.

address	name	Bit width	default value	describe
D	I[1]_RMS	twenty four	0x000000	Current1Channel RMS register
E	I[2]_RMS	twenty four	0x000000	Current2Channel RMS register

F	I[3]_RMS	twenty four	0x000000	Current3Channel RMS register
10	I[4]_RMS	twenty four	0x000000	Current4Channel RMS register
13	I[5]_RMS	twenty four	0x000000	Current5Channel RMS register
14	I[6]_RMS	twenty four	0x000000	Current6Channel RMS register
16	V_RMS	twenty four	0x000000	Voltage channel effective value register

When a channel is in anti-submarine state, the effective value of the channel is not measured.

Current RMS register value:$I\_RMS = \frac{12875 \times I(A) \times Gain\_I}{Vref}$

Voltage RMS register value:$V\_RMS = \frac{13162 \times V(V) \times Gain\_V}{Vref}$

Vrefis the reference voltage, the typical value is1.097V.

I(A),V(V)The voltage signal of the current and voltage input pin (unit:mV);

Gain_I,Gain_Vis the corresponding channel gain multiple;

Setting of effective value input signal

The waveforms for calculating effective values are divided into full wave, AC full wave, fundamental wave and DC.HPFOutput full-wave waveform. HPFIn AC measurement mode, it outputs AC full-wave waveform.LPFIn fundamental wave measurement mode, output fundamental wave waveform.LPFIn DC measurement mode, it outputs DC waveform.MODE2To set up, each channel can be set up separately.

0x97	MODE2	Working Mode Register	
No.	name	default value	description
[21:0]	WAVE_RMS_SEL	11{2'b00}	RMS waveform selection,00-AC full wave,10-DC,01-Fundamental wave, 11-Full Wave [3:2]: Current1aisle;[5:4]: Current2aisle; [7:6]: Current3aisle;[9:8]: Current4aisle; [15:14]: Current5aisle;[17:16]: Current6aisle; [21:20]: Voltage channel

3.4.2RMS value & power refresh rate settings

set upMODE2[22]ofRMS_UPDATE_SEL, you can choose the effective value & power average refresh time is 525ms or105ms,default500ms.

0x97	MODE2	Working Mode Register

No.	name	default value	description
[twenty two]	RMS_UPDATE_SEL	1'b0	Effective value memory update speed selection,1-105ms,0-525ms, the default selection525ms

3.4.3Current and voltage RMS calibration

Included7indivualtwenty fourValid value offset correction registerRMSOS[N]and7indivual161-bit RMS gain correction registerRMSGN[N], the default value is0000H.

They2The data in the form of two's complement is used to calibrate the deviation in the effective value calculation. This deviation may come from input noise, because there is a square operation in the calculation of the effective value, which may introduce a DC offset caused by noise. Gain and offset correction can make the value in the effective value register close to0.

address	name	Bit width	default value	describe
6D	RMSGN[1]	16	0x0000	Current1Channel RMS gain adjustment register
6E	RMSGN[2]	16	0x0000	Current2Channel RMS gain adjustment register
6F	RMSGN[3]	16	0x0000	Current3Channel RMS gain adjustment register
70	RMSGN[4]	16	0x0000	Current4Channel RMS gain adjustment register
73	RMSGN[5]	16	0x0000	Current5Channel RMS gain adjustment register
74	RMSGN[6]	16	0x0000	Current6Channel RMS gain adjustment register
76	RMSGN[V]	16	0x0000	Voltage channel RMS gain adjustment register
78	RMSOS[1]	twenty four	0x000000	Current1Channel RMS offset correction register
79	RMSOS[2]	twenty four	0x000000	Current2Channel RMS offset correction register
7A	RMSOS[3]	twenty four	0x000000	Current3Channel RMS offset correction register
7B	RMSOS[4]	twenty four	0x000000	Current4Channel RMS offset correction register
7E	RMSOS[5]	twenty four	0x000000	Current5Channel RMS offset correction register
7F	RMSOS[6]	twenty four	0x000000	Current6Channel RMS offset correction register
81	RMSOS[V]	twenty four	0x000000	Voltage channel RMS offset correction register

Calibration formula:

$$RMS[N] = \sqrt{RMS[N]_0^2 + RMSOS[N]\text{-}256}$$

hereRMS[N]0For theNThe effective value of the channel before calibration.RMS[N]It isNThe effective value of the channel after calibration.

3.4.4Effective value anti-creep

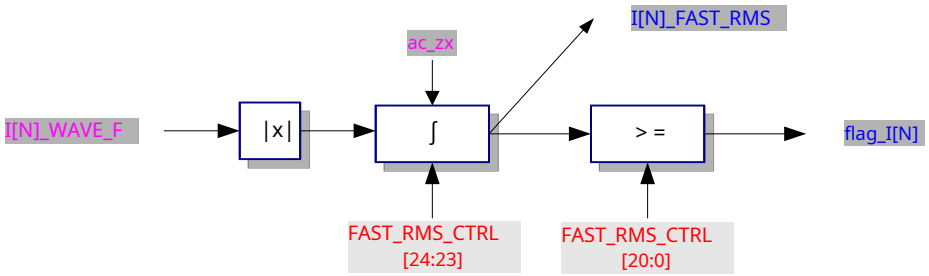
With patented RMS anti-submarine function, it ensures that the RMS output is0.

Effective value anti-creep threshold register (RMS_CREEP),for12bitUnsigned number, default is0x200The value is internally expanded2After multiplying the value, it is compared with the absolute value of the input effective value signal. When the input effective value signal is less than this value, the output effective value is set to zero. This can make the value output to the effective value register equal to zero even if there is a small noise signal in the no-load condition.0.

address	name	Bit width	default value	describe
8A	RMS_CREEP	12	0x200	RMS small signal threshold register

3.5Fast effective value detection principle

The principle of fast effective value calculation is shown in the figure below.



7Each channel has a fast RMS register that can detect half-cycle or cycle RMS. This function can be used for leakage or overcurrent detection.

The input waveform is taken in absolute value and then integrated within a specified time to obtain a fast effective value. This value can be compared with a pre-set threshold and a flag can be given if it exceeds.

3.5.1Fast RMS output

7The fast effective value output register of the channel is shown in the figure below. This register istwenty fourUnsigned bit number.

address	name	Bit width	default value	describe
18	I[1]_FAST_RMS	twenty four	0x000000	Current1Channel fast RMS register
19	I[2]_FAST_RMS	twenty four	0x000000	Current2Channel fast RMS register
1A	I[3]_FAST_RMS	twenty four	0x000000	Current3Channel fast RMS register

1B	I[4]_FAST_RMS	twenty four	0x000000	Current4Channel fast RMS register
1E	I[5]_FAST_RMS	twenty four	0x000000	Current5Channel fast RMS register
1F	I[6]_FAST_RMS	twenty four	0x000000	Current6Channel fast RMS register
twenty one	V_FAST_RMS	twenty four	0x000000	Voltage channel fast RMS register

3.5.2Fast RMS input selection

The waveforms for fast effective value calculation are divided into full wave and AC full wave.HPFOutput full-wave waveform.HPF In AC measurement mode, it outputs AC full-wave waveform.MODE1[22]to set it up.

0x96	MODE1	Working Mode Register	
No.	name	default value	description
[twenty two]	L_F_SEL	1'b0	Fast effective value calculation selects high pass, the default is0-No Qualcomm,1-Choose Qualcomm

3.5.3Fast RMS accumulation time and threshold

To calculate the fast effective value, first take the absolute value, then integrate it according to the set cumulative time. Generally, take the integer multiple of half cycle or cycle time.

address	name	Bit width	default value	describe
8B	FAST_RMS_CTRL	twenty four	0x20FFFF	[23:21]Channel fast effective value register refresh time, selectable half cycle andNFrequency, default is1Zhou Bo; [20:0]Pass Fast RMS Threshold Register

Depend onFAST_RMS_CTRL[23:21]Select the accumulated time.000-10ms,001-20ms,010-40ms,011- 80ms,100-160ms, 101-320msThere are six types in total, and the default selection is cycle cumulative response time20msThe longer the accumulated time, the smaller the jump.

FAST_RMS_CTRL[20:0]Used to set the fast effective value exceeding the limit threshold. Once exceeded, the output flagflag[N] for1. Flag bit connection output (M1~M6), you can directly pull the overcurrent output indication pin high. It can be used in conjunction with the overcurrent indication control register.

3.5.4Grid frequency selection

passAC_FREQ_SELRegisters can be distinguished50Hzand60Hzpower grid applications.

0x97	MODE2	Working Mode Register

No.	name	default value	description
[twenty three]	AC_FREQ_SEL	1'b0	AC frequency selection: 1-60Hz;0-50Hz, the default selection50Hz

3.5.5Fast effective value exceeding limit data storage

In order to record the fast overload signal, the fast effective value over limit has a saving function, and certain setting operations are required to clear the relevant registersI[N]_FAST_RMS_HOLD. See the table below for specific registers:

address	name	Bit width	default value	describe
47	I[1]_FAST_RMS_HOLD	twenty four	0x000000	Current1Channel fast effective value register, unsigned No., keep
48	I[2]_FAST_RMS_HOLD	twenty four	0x000000	Current2Channel fast effective value register, unsigned No., keep
49	I[3]_FAST_RMS_HOLD	twenty four	0x000000	Current3Channel fast effective value register, unsigned No., keep
57	I[4]_FAST_RMS_HOLD	twenty four	0x000000	Current4Channel fast effective value register, unsigned No., keep
5A	I[5]_FAST_RMS_HOLD	twenty four	0x000000	Current5Channel fast effective value register, unsigned No., keep
5B	I[6]_FAST_RMS_HOLD	twenty four	0x000000	Current6Channel fast effective value register, unsigned No., keep

3.5.6Overcurrent indication

Overcurrent indication (M1~M6) can be controlled by the following overcurrent indication control register:

address	name	Bit width	default value	describe
91	flag_ctrl1	twenty four	0x000000	Overcurrent indication control register1. [23:10]Disconnect delay timer,0.1ms/lsb; [9:0]Indicator control,M1-M6:0-Output real-time interrupt;1-Output delay control [1]: Current1aisle;[2]: Current2aisle; [3]: Current3aisle;[4]: Current4aisle; [7]: Current5aisle;[8]: Current6aisle
92	flag_ctrl2	twenty four	0x000000	Overcurrent indication control register2.

				[23:10]Closing delay timer,0.1ms/lsb; [9:0]Closed control,M1-M6:0-closure,1-disconnect [1]: Current1aisle;[2]: Current2aisle; [3]: Current3aisle;[4]: Current4aisle; [7]: Current5aisle;[8]: Current6aisle

3.5.7Relay control

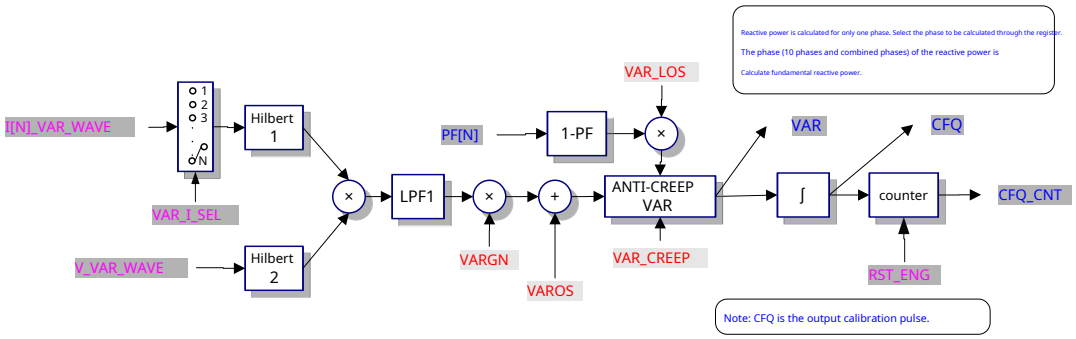
You can also write registers directlyflag_ctrlTo directly controlM1~M6The output level of the pin is used for relay control system:

address	name	Bit width	default value	describe
90	flag_ctrl	twenty four	0x000000	Master direct controlM1~M6Output level status [1]: Current1aisle;[2]: Current2aisle; [3]: Current3aisle;[4]: Current4aisle; [7]: Current5aisle;[8]: Current6aisle

Bit[21:12]is the control priority of the output;

3.6Reactive power calculation

The reactive power calculation principle is shown in the figure below.



The current and voltage waveforms areHillbertAfter the filter, digital multiplication is performed, and then the reactive power signal can be obtained after the low-pass filter, gain and deviation calibration, anti-creep judgment and average processing in sequence. After integration, the reactive energy pulse accumulation is obtained.

3.6.1Reactive power calculation input selection

Input can beVAR_I_SELRegister Selection6One of the currents multiplied by the voltage

0x98	MODE3	Working Mode Register	
No.	name	default value	description
[3:0]	VAR_I_SEL	4'b000	Select the reactive current measurement channel,6select1,default0000 0001-aisle1;0010-aisle2;0011-aisle3; 0100-aisle4;0111-aisle5;1000-aisle6.

3.6.2Phase compensation

Adjustable phase compensation of current and voltage channels for reactive power calculation, phase calibration register VAR_PHCAL_Iand VAR_PHCAL_VThe data format is as follows (reactive phase correction (fine tuning)fine-tuning, the minimum adjustment delay time between500ns,correspond0.009Spend/1LSB, maximum adjustable ±0.072Spend.):

address	name	Bit width	default value	describe
6A	VAR_PHCAL_I	5	0000H	Current channel reactive phase correction
6B	VAR_PHCAL_V	5	0000H	Voltage channel reactive phase correction

3.6.3Reactive power output

Output only1Phase reactive power, fundamental reactive power and total reactive power are given separately.

address	name	Bit width	default value	describe
2D	VAR	twenty four	0x000000	Optional channel reactive power register (fundamental)
5D	VAR	twenty four	0x000000	Optional channel reactive power register (full wave)

3.6.4Reactive power calibration

Included1indivual16Reactive Bias Correction RegisterVAROSand1indivual16Reactive Gain Correction Register VARGN, the default value is0000H.

They2The data in the form of the two's complement is used to calibrate the deviation in the reactive power calculation. This deviation may come from input noise or phase difference, which may introduce DC offset and gain errors caused by noise. Gain and offset correction can correct the reactive power measurement curve.

address	name	Bit width	default value	describe
CA	VARGN	16	0x0000	Corresponding channel reactive power gain adjustment register, complement code

CB	VAROS	16	0x0000	Corresponding channel reactive power bias adjustment register, complement code

3.6.5Reactive power anti-creep

Patented power anti-submarine function ensures that the power output is0.

Reactive power anti-creep threshold register (VAR_CREEP),for12bitUnsigned number, default is0x04CThe value is internally expanded1After multiplying, it is compared with the absolute value of the input reactive power signal. When the absolute value of the input reactive power signal is less than this value, the output reactive power is set to zero. This allows the value output to the reactive power register to be zero even if there is a small noise signal in the case of reactive power measurement.0.

address	name	Bit width	default value	describe
88	VAR_CREEP/ WA_CREEP	twenty four	0x04C04C	[11:0]Active anti-creep power threshold register WA_CREEP;[23:12]Reactive power protection threshold MemoryVAR_CREEP.

The power registerVARValue SettingVAR_CREEP, their corresponding relationship, the anti-submarine value is generally taken as 20 millionths to 200 millionths of the full scale of reactive power.

When a channel is in the anti-submarine state, the power of the channel below the threshold does not participate in energy accumulation.

3.6.6Reactive power small signal compensation

For reactive power calculation, in order to reduce the noise error in the small signal segment, the small signal compensation register can be used to adjust the nonlinear error of the small signal segment.

address	name	Bit width	default value	describe
87	VAR_LOS/FVAR_LOS	twenty four	0x000000	[11:0]Corresponding reactive (fundamental wave) small signal compensation register Device, complement.23:12]Corresponding reactive small signal compensation register Device, complement.

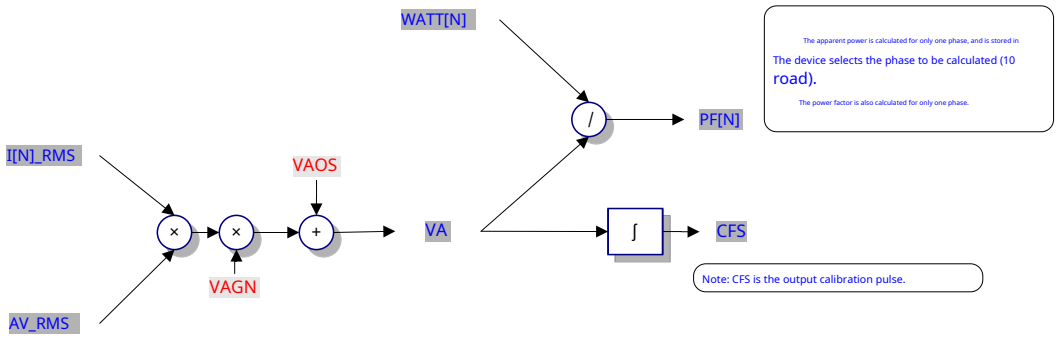
3.6.7Reactive energy output

ReactiveCFThe pulse counting can obtain the reactive energy and store it in the reactive energy accumulation register.CFQ_CNT.

address	name	Bit width	default value	describe
3A	CFQ_CNT	twenty four	0x000000	Optional channel reactive energy pulse count, unsigned (fundamental wave)

3.7Apparent and power factor calculations

The apparent calculation principle is shown in the figure below



The current and voltage RMS values are digitally multiplied, and then the gain and offset calibrations are performed in sequence to obtain the reactive power signal. After integration, the reactive energy pulse accumulation is obtained. The active power is divided by the apparent power to obtain the power factor.

3.7.1Apparent power and energy output

Output only1The apparent power and energy of the road are given byMODE3（VAR_I_SEL) register selection, that is, which channel is selected reactively and which channel is also selected apparently.

address	name	Bit width	default value	describe
2E	VA	twenty four	0x000000	Selectable channel apparent power register
3B	CFS_CNT	twenty four	0x000000	Optional channel apparent energy pulse count, unsigned

3.7.2Apparent power calibration

Included1indivual16The apparent bias correction registerVAOSand1indivual16The apparent gain correction register VAGN, the default value is0000H.

They2The data in the form of the two's complement is used to calibrate the deviation in the apparent calculation. This deviation may come from the previous stage, which may introduce offset and gain errors. Gain and offset correction can correct the apparent measurement curve.

address	name	Bit Width	default value	describe
CC	VAGN	16	0x0000	Corresponding channel apparent power gain adjustment register, complement code
CD	VAOS	16	0x0000	Corresponding channel apparent power bias adjustment register, complement code

3.7.3Power Factor

Output only1The power factor is given byMODE3（VAR_I_SEL) register selection, that is, which channel is selected for reactive power and which channel is also selected for power factor.

address	name	Bit width	default value	describe
4A	PF	twenty four	0x000000	Selectable channel power factor register

3.8Temperature measurement

Provides internal temperature measurement.

Internal temperature readings are stored inTPSregister.

address	name	Bit width	default value	describe
5E	TPS	10	0x000000	Internal temperature value register

Internal temperature measurement formula: internal temperature = (TPS-64)*12.5/59-40(℃)

3.9Electrical parameter measurement

3.9.1Line cycle metering

It has a line cycle energy accumulation calculator, including active and reactive power.

address	name	Bit width	default value	describe
4B	LINE_ WATTHR	twenty four	0	Line cycle accumulated active energy register
4C	LINE_ VARHR	twenty four	0	Line cycle accumulated reactive energy register

The number of line cycles can be determined byLINECYCRegister Selection:

address	name	Bit width	default value	describe
8F	SAGLVL/ LINECYC	twenty four	0x100009	[[11:0]Line energy accumulation cycle number registerLINECYC, default009H,represent10cycle.

3.9.2Line frequency measurement

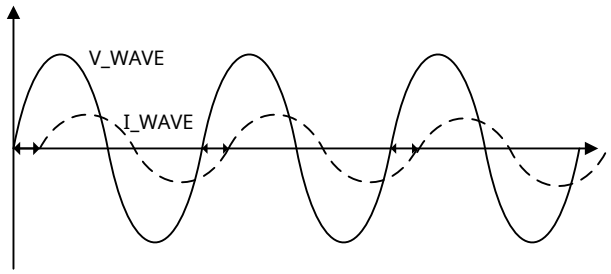
For grid frequency test, voltage channel test.

PERIODThe count of line cycles recorded in the register, if the input signal deviates from50Hz/60Hz, the corresponding count value will change.

address	name	Bit width	default value	describe
4E	PERIOD	20	0x000000	Line voltage frequency period register

3.9.3Phase angle calculation

Phase angle measurement principle, see the figure below



The phase difference is obtained by calculating the time difference between the positive zero crossing of the current and voltage, and the corresponding time value is updated to the register ANGLE[N], each register is16Unsigned bit number.

address	name	Bit width	default value	describe
3D	ANGLE[1]	16	0x000000	aisle1Current and voltage waveform angle register
3E	ANGLE[2]	16	0x000000	aisle2Current and voltage waveform angle register
3F	ANGLE[3]	16	0x000000	aisle3Current and voltage waveform angle register
40	ANGLE[4]	16	0x000000	aisle4Current and voltage waveform angle register
43	ANGLE[5]	16	0x000000	aisle5Current and voltage waveform angle register
44	ANGLE[6]	16	0x000000	aisle6Current and voltage waveform angle register

3.9.4Power sign bit

For each channel power pulseCFOutput, signed bit register, indicating eachCFThe direction indicates the direction from the previousCFTo the presentCF During the pulse process, the corresponding direction of the accumulated energy (power consumption or power supply).

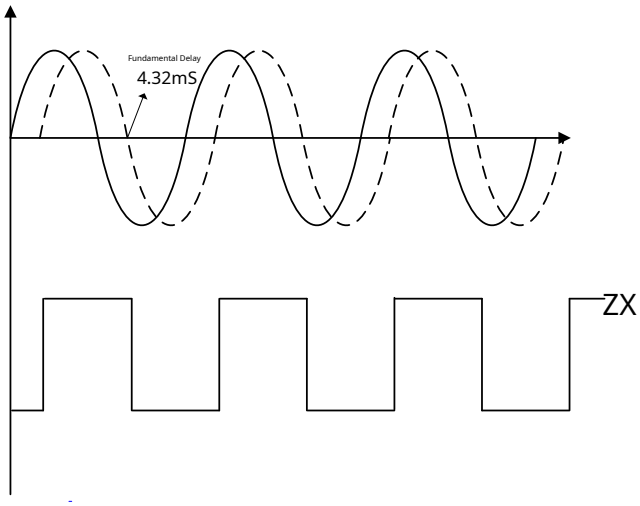
address	name	Bit width	default value	describe
4D	SIGN	twenty four	0x000000	Power sign bit. Corresponding to the sign bit of the current energy pulse count,CFpulse Refresh when. [1]:1Channel active;2]:2Channel active;3]:3The channel is active; [4]:4Channel active;7]:5Channel active;8]:6The channel is active; [10]：Combined with merit;11]: Optional reactive power;

3.10Fault Detection

3.10.1Zero Crossing Detection

Provides voltage zero-crossing detection by pinZXDirectly output zero-crossing signal,ZXZero indicates the positive half cycle of the waveform.ZXfor 1Indicates the negative half cycle of the waveform. The chip detects the fundamental zero-crossing signal, which passes through the fundamental filter and has a time delay with the actual input signal.4.32mSabout.

The output zero-crossing signal mainly assists in shutting off the relay at the zero-crossing point to reduce the relay sticking phenomenon.



Note: To prevent the uncertainty caused by the presence of stray signals in the background noise signal or small signal, the current zero-crossing threshold is 70000, the voltage zero crossing threshold is200000.If the instantaneous effective value is smaller than the threshold,ZXSignal.

3.10.2Peak value exceeded

The current and voltage RMS thresholds can be set by the peak threshold register (I_PKLVL,V_PKLVL)set up Certainly.

address	name	Bit width	default value	describe

8C	I_PKLVL/V_PKL V L	twenty four	0xFFFFFF	[23:12]Current Peak Threshold RegisterI_PKLVL; [11:0]Voltage Peak Threshold RegisterV_PKLVL

For example: when the channel1The current fast effective value is greater than the current peak threshold register (I_PKLVL) when the set threshold is exceeded, an overload indication is givenPK01.

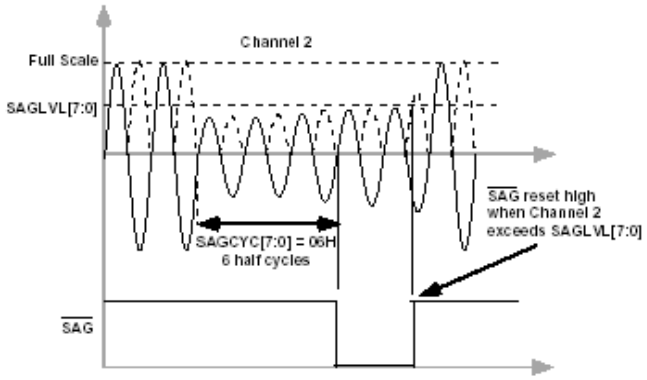
Likewise, when the channel2~6The current RMS value is greater than the current peak threshold register (I_PKLVL) when the set threshold is exceeded, an overload indication is givenPK02~PK06.

Similarly, when the voltage fast effective value is greater than the voltage peak threshold register (V_PKLVL) when the set threshold is exceeded, a voltage overload indication is givenPKV.

0x96	STATUS1		
Location	Interrupt flag	default value	describe
14	pk01	0	Current1Channel peak value exceeding limit signal
15	pk02	0	Current2Channel peak value exceeding limit signal
16	pk03	0	Current3Channel peak value exceeding limit signal
17	pk04	0	Current4Channel peak value exceeding limit signal
20	pk05	0	Current5Channel peak value exceeding limit signal
twenty one	pk06	0	Current6Channel peak value exceeding limit signal
twenty three	pkv	0	Voltage channel peak value exceeding limit signal

3.10.3Line voltage drop

When the effective value of the line voltage is lower than a certain peak value for more than a certain number of half cycles, a line voltage drop indication is given.



As shown in the figure above, when the voltage RMS value is less than the drop voltage threshold register (SAGLVL) and the fall time exceeds the fall line period register (SAGCYC) (the figure shows the time exceeded6Half cycle

back,SAGCC[11:0]=06H）, the line voltage drop event is interrupted by setting theSTATUS1RegisterSAG Flag to record it.

0x96	STATUS1		
Location	Interrupt flag	default value	describe
0	sag	0	Line voltage drop

The number of drop cycles and the drop voltage threshold can be set. The drop voltage threshold register (SAGLVL) can be written or read by the user, the initial value is0x100, drop line cycle register (SAGCYC) can also be written or read by the user, the initial value is0x04.

address	name	Bit width	default value	describe
8E	SAGCYC/ZX TOUT	twenty four	0x04FFFF	[23:16]Drop Line Period RegisterSAGCYC,default04H.
8F	SAGLVL/LI NECYC	twenty four	0x100009	[23:12]Falling voltage threshold registerSAGLVL, the voltage channel input is continuously lower than the value of this register for more thanSAGCYCThe time in which the line voltage drops will be interrupted will be generated. The default value is100H,about1/16Full Degree voltage input.

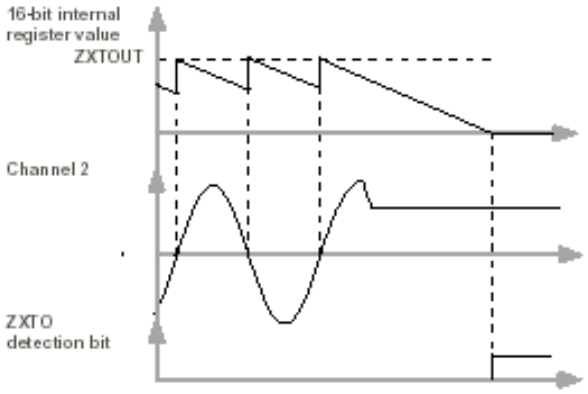
3.10.4Zero crossing timeout

The zero-crossing detection circuit is also connected to a register that detects the zero-crossing signal timeout.ZXTOUT, whenever the detection voltage channel has a zero-crossing signalZXTOUTIf there is no zero-crossing signal, it will decrease. If there is no zero-crossing signal output for a long time, the value in the register will become0, then the corresponding bit in the interrupt status registerZXTOPlaced1

address	name	Bit width	default value	describe
8E	SAGCYC/ZX TOUT	twenty four	0x04FFFF	[15:0]Zero Crossing Timeout RegisterZXTOUTIf there is no zero-crossing signal within the time indicated by this register, a zero-crossing timeout interrupt will be generated. ProvinceFFFFH.

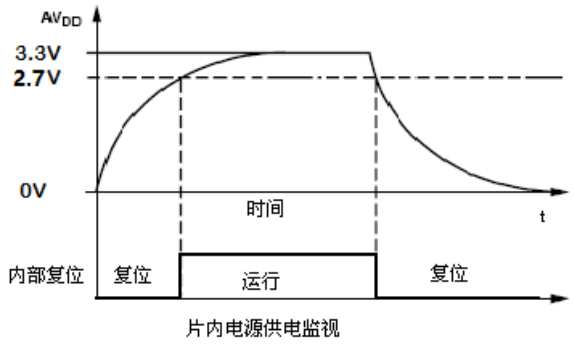
Zero Crossing Timeout RegisterZXTOUTCan be written or read by the user, the initial value is0xFFFFThe resolution of this register is64us/ LSB, so that the maximum delay time of an interrupt is limited to4.26s.

The following figure shows the mechanism of detecting zero-crossing timeout when the line voltage is always a fixed DC signal:



3.10.5Power supply indication

Contains an on-chip power supply monitoring circuit that continuously monitors the analog power supply (VDD). If the power supply voltage is less than 2.7V±5%, the entire circuit is not activated (does not work), that is, when the power supply voltage is less than2.7VWhen the power supply is turned on or off, no energy accumulation is performed. This approach ensures that the device maintains correct operation when the power supply is turned on or off. This power monitoring circuit has a hysteresis and filtering mechanism that can largely eliminate false triggers caused by noise. In general, the decoupling part of the power supply should be ensured inVDDThe ripples on the3.3V-5%.



片内电源供电监视

3.10.6 ADCShutdown

address	name	Bit width	default value	describe
93	ADC_PD	11	0x000	7ChannelsADCEnable control: [0]-Voltage channel; [2]-1aisle; [3]-2aisle;[4]-3aisle; [5]-4aisle;[8]-5aisle; [9]-6aisle;

The bit setting bit of the corresponding channel1When not in use, the channels that do not need to work are turned off to reduce power consumption.

[10:0]Undescribed reserved bits in the1;

4.Internal Registers

4.1Electrical parameter register (read only)

address	name	Bit width	default value	describe
1	reserve			
2	I[1]_WAVE	twenty four	0x000000	Current1Channel waveform registers (normal current and fast (speed current optional)
3	I[2]_WAVE	twenty four	0x000000	Current2Channel waveform registers (normal current and fast (speed current optional)
4	I[3]_WAVE	twenty four	0x000000	Current3Channel waveform registers (normal current and fast (speed current optional)
5	I[4]_WAVE	twenty four	0x000000	Current4Channel waveform registers (normal current and fast (speed current optional)
6	reserve			
7	reserve			
8	I[5]_WAVE	twenty four	0x000000	Current5Channel waveform registers (normal current and fast (speed current optional)
9	I[6]_WAVE	twenty four	0x000000	Current6Channel waveform registers (normal current and fast (speed current optional)
A	reserve			
B	V_WAVE	twenty four	0x000000	Voltage channel waveform register
C	reserve			
D	I[1]_RMS	twenty four	0x000000	Current1Channel RMS register
E	I[2]_RMS	twenty four	0x000000	Current2Channel RMS register
F	I[3]_RMS	twenty four	0x000000	Current3Channel RMS register
10	I[4]_RMS	twenty four	0x000000	Current4Channel RMS register
11	reserve			
12	reserve			
13	I[5]_RMS	twenty four	0x000000	Current5Channel RMS register
14	I[6]_RMS	twenty four	0x000000	Current6Channel RMS register
15	reserve			

16	V_RMS	twenty four	0x000000	Voltage channel effective value register
17	reserve			
18	I[1]_FAST_RMS	twenty four	0x000000	Current1Channel fast RMS register
19	I[2]_FAST_RMS	twenty four	0x000000	Current2Channel fast RMS register
1A	I[3]_FAST_RMS	twenty four	0x000000	Current3Channel fast RMS register
1B	I[4]_FAST_RMS	twenty four	0x000000	Current4Channel fast RMS register
1C	reserve			
1D	reserve			
1E	I[5]_FAST_RMS	twenty four	0x000000	Current5Channel fast RMS register
1F	I[6]_FAST_RMS	twenty four	0x000000	Current6Channel fast RMS register
20	reserve			
twenty one	V_FAST_RMS	twenty four	0x000000	Voltage channel fast RMS register
twenty two	reserve			
twenty three	WATT[1]	twenty four	0x000000	aisle1Active Power Register
twenty four	WATT[2]	twenty four	0x000000	aisle2Active Power Register
25	WATT[3]	twenty four	0x000000	aisle3Active Power Register
26	WATT[4]	twenty four	0x000000	aisle4Active Power Register
27	reserve			
28	reserve			
29	WATT[5]	twenty four	0x000000	aisle5Active Power Register
2A	WATT[6]	twenty four	0x000000	aisle6Active Power Register
2B	reserve			
2C	WATT	twenty four	0x000000	Total active power register
2D	VAR	twenty four	0x000000	Optional channel reactive power register (fundamental)
2E	VA	twenty four	0x000000	Selectable channel apparent power register
2F	reserve			
30	CF[1]_CNT	twenty four	0x000000	aisle1Active energy pulse counting
31	CF[2]_CNT	twenty four	0x000000	aisle2Active energy pulse counting

32	CF[3]_CNT	twenty four	0x000000	aisle3Active energy pulse counting
33	CF[4]_CNT	twenty four	0x000000	aisle4Active energy pulse counting
34	reserve			
35	reserve			
36	CF[5]_CNT	twenty four	0x000000	aisle5Active energy pulse counting
37	CF[6]_CNT	twenty four	0x000000	aisle6Active energy pulse counting
38	reserve			
39	CF_CNT	twenty four	0x000000	Total active energy pulse count
3A	CFQ_CNT	twenty four	0x000000	Optional channel reactive energy pulse counting
3B	CFS_CNT	twenty four	0x000000	Optional channel apparent energy pulse counting
3C	reserve			
3D	ANGLE[1]	16	0x000000	aisle1Current and voltage waveform angle register
3E	ANGLE[2]	16	0x000000	aisle2Current and voltage waveform angle register
3F	ANGLE[3]	16	0x000000	aisle3Current and voltage waveform angle register
40	ANGLE[4]	16	0x000000	aisle4Current and voltage waveform angle register
41	reserve			
42	reserve			
43	ANGLE[5]	16	0x000000	aisle5Current and voltage waveform angle register
44	ANGLE[6]	16	0x000000	aisle6Current and voltage waveform angle register
45	reserve			
46	reserve			
47	I[1]_FAST_RMS_HOLD	twenty four	0x000000	Current1Channel fast effective value register, unsigned No., keep
48	I[2]_FAST_RMS_HOLD	twenty four	0x000000	Current2Channel fast effective value register, unsigned No., keep
49	I[3]_FAST_RMS_HOLD	twenty four	0x000000	Current3Channel fast effective value register, unsigned No., keep
4A	PF	twenty four	0x000000	Selectable channel power factor register
4B	LINE_ WATTHR	twenty four	0x000000	Line cycle accumulated active energy register

4C	LINE_ VARHR	twenty four	0x000000	Line cycle accumulated reactive energy register
4D	SIGN	twenty four	0x000000	Power sign bit. Corresponding to the current energy pulse count The sign bit isCFRefresh on pulse
4E	PERIOD	20	0x000000	Line voltage frequency period register (optional channel)
4F	reserve			
50	reserve			
51	reserve			
52	reserve			
53	reserve			
54	STATUS1	twenty four	0x000000	Interrupt Status Register1
55	reserve			
56	STATUS3	10	0x000	MStatus Register
57	I[4]_FAST_RMS_HOLD	twenty four	0x000000	Current4Channel fast effective value register, unsigned No., keep
58	reserve			
59	reserve			
5A	I[5]_FAST_RMS_HOLD	twenty four	0x000000	Current5Channel fast effective value register, unsigned No., keep
5B	I[6]_FAST_RMS_HOLD	twenty four	0x000000	Current6Channel fast effective value register, unsigned No., keep
5C	reserve			
5D	VAR	twenty four	0x000000	Selectable channel (full wave) reactive power register
5E	TPS	10	0x000000	Internal temperature value register
5F	reserve			

4.2Calibration register1

land site	name	Bit Width	default value	describe
60	GAIN1	twenty four	0x000000	aislePGAGain Adjust Register [3:0]: Voltage channel

				[11:8]: Current1aisle [15:12]: Current2aisle [19:16]: Current3aisle [23:20]: Current4aisle
61	GAIN2	20	0x00000	aislePGAGain Adjust Register [11:8]: Current5aisle [15:12]: Current6aisle
62	reserve			
63	reserve			
64	NA/ PHASE[1]	16	0x0000	[15:8]:reserve [7:0]: Current1aisle
65	PHASE[2]/ PHASE[3]	16	0x0000	[15:8]: Current2aisle [7:0]: Current3aisle
66	PHASE[4]/ NA	16	0x0000	[15:8]: Current4aisle [7:0]:reserve
67	NA/ PHASE[5]	16	0x0000	[15:8]:reserve [7:0]: Current5aisle
68	PHASE[6]/ NA	16	0x0000	[15:8]: Current6aisle [7:0]:reserve
69	PHASE[V]	8	0x00	Voltage Channel
6A	VAR_PHCAL_I	5	0x00	Current channel reactive phase correction
6B	VAR_PHCAL_V	5	0x00	Voltage channel reactive phase correction
6C	reserve			
6D	RMSGN[1]	16	0x0000	Current1Channel RMS gain adjustment register
6E	RMSGN[2]	16	0x0000	Current2Channel RMS gain adjustment register
6F	RMSGN[3]	16	0x0000	Current3Channel RMS gain adjustment register
70	RMSGN[4]	16	0x0000	Current4Channel RMS gain adjustment register
71	reserve			
72	reserve			
73	RMSGN[5]	16	0x0000	Current5Channel RMS gain adjustment register
74	RMSGN[6]	16	0x0000	Current6Channel RMS gain adjustment register

75	reserve			
76	RMSGN[V]	16	0x0000	Voltage channel RMS gain adjustment register
77	reserve			
78	RMSOS[1]	twenty four	0x000000	Current1Channel RMS offset correction register
79	RMSOS[2]	twenty four	0x000000	Current2Channel RMS offset correction register
7A	RMSOS[3]	twenty four	0x000000	Current3Channel RMS offset correction register
7B	RMSOS[4]	twenty four	0x000000	Current4Channel RMS offset correction register
7C	reserve			
7D	reserve			
7E	RMSOS[5]	twenty four	0x000000	Current5Channel RMS offset correction register
7F	RMSOS[6]	twenty four	0x000000	Current6Channel RMS offset correction register
80	reserve			
81	RMSOS[V]	twenty four	0x000000	Voltage channel RMS offset correction register
82	reserve/ WA_LOS[1]	twenty four	0x000000	[23:12]:reserve [11:0]:aisle1Active power small signal compensation register
83	WA_LOS[2]/ WA_LOS[3]	twenty four	0x000000	[23:12]:aisle2Active power small signal compensation register [11:0]:aisle3Active power small signal compensation register
84	WA_LOS[4]/ reserve	twenty four	0x000000	[23:12]:aisle4Active power small signal compensation register [11:0]:reserve
85	reserve/ WA_LOS[5]	twenty four	0x000000	[23:12]:reserve [11:0]:aisle5Active power small signal compensation register
86	WA_LOS[6]/ reserve	twenty four	0x000000	[23:12]:aisle6Active power small signal compensation register [11:0]:reserve
87	VAR_LOS/ FVAR_LOS	twenty four	0x000000	[11:0]Corresponding to reactive (fundamental) small signal compensation register, complement code.23:12]Corresponding to the reactive small signal compensation register, complement code.
88	VAR_CREEP/ WA_CREEP	twenty four	0x04C04C	[11:0]Active anti-creep power threshold register WA_CREEP;[23:12]Reactive power protection threshold MemoryVAR_CREEP.
89	WA_CREEP2	12	0x000	[11:0]Total active power anti-creep threshold register
8A	RMS_CREEP	12	0x200	RMS small signal threshold register

8B	FAST_RMS_CTRL	twenty four	0x20FFFF	[23:21]Channel fast effective value register refresh time, selectable half cycle andNFrequency, the default is frequency; [20:0]Fast channel Validity Threshold Register
8C	I_PKLVL/ V_PKLVL	twenty four	0xFFFFFF	[23:12]Current Peak Threshold RegisterI_PKLVL; [11:0]electricity Voltage Peak Threshold RegisterV_PKLVL
8D	reserve			
8E	SAGCYC/ ZXTOUT	twenty four	0x04FFFF	[23:16]Drop Line Period RegisterSAGCYC,default04H; [15:0]Zero Crossing Timeout RegisterZXTOUTIf there is no zero-crossing signal within the time indicated by this register, a zero-crossing timeout will occur. Interrupt, defaultFFFFH.
8F	SAGLVL/ LINECYC	twenty four	0x100009	[23:12]Falling voltage threshold registerSAGLVL, the voltage channel input is continuously lower than the value of this register for more thanSAGCYC The line voltage drop interruption will occur during the time. The default value is 100H,about1/16Full voltage input; [11:0]Line energy accumulation cycle number registerLINECYC,default009H,represent10 cycle.
90	flag_ctrl	twenty four	0x000000	Master direct controlM1~M6Output level status
91	flag_ctrl1	twenty four	0x000000	Overcurrent indication control register1. [23:10]Disconnect delay timer,0.1ms/lsb; [9:0]Indicator control,M1-M6:0-Output real-time interrupt;1-lose Output delay control [1]: Current1aisle;[2]: Current2aisle; [3]: Current3aisle;[4]: Current4aisle; [7]: Current5aisle;[8]: Current6aisle
92	flag_ctrl2	twenty four	0x000000	Overcurrent indication control register2. [23:10]Closing delay timer,0.1ms/lsb; [9:0]Closed control,M1-M6:0-closure,1-disconnect [1]: Current1aisle;[2]: Current2aisle; [3]: Current3aisle;[4]: Current4aisle; [7]: Current5aisle;[8]: Current6aisle
93	ADC_PD	11	0x000	7ChannelsADCEnable control: [0]-Voltage channel; [2]-Current1aisle;[3]-Current2aisle;[4]-Current3aisle;[5]-Current4aisle;[8]-Current5aisle;[9]-Current6 aisle
94	reserve			
95	reserve			
96	MODE1	twenty four	0x000000	User Mode Select Register1

97	MODE2	twenty four	0x000000	User Mode Select Register2
98	MODE3	twenty four	0x000000	User Mode Select Register3
99	reserve			
9A	reserve			
9B	reserve			
9C	reserve			
9D	RST_ENG	twenty four	0x000000	Energy reset setting register, see "Energy reset setting register Device" Description
9E	USR_WRPROT	16	0x00	User write protection setting register, write5555HWhen , it indicates that the user register pair can be operatedreg60arrivereg9d,rega0arrived0
9F	SOFT_RESET	twenty four	0x000000	When the input is5A5A5AWhen the system is reset - only the digital Part of the state machine and registers! When the input is55AA55When the user reads and writes the registers, they are reset. Reset:reg60arrivereg9f,rega0arriveregd0

4.3Calibration register2

address	name	Bit width	default value	describe
A0	reserve			
A1	CHGN[1]	16	0x0000	Current1Channel gain adjustment register, two's complement
A2	CHGN[2]	16	0x0000	Current2Channel gain adjustment register, two's complement
A3	CHGN[3]	16	0x0000	Current3Channel gain adjustment register, two's complement
A4	CHGN[4]	16	0x0000	Current4Channel gain adjustment register, two's complement
A5	reserve			
A6	reserve			
A7	CHGN[5]	16	0x0000	Current5Channel gain adjustment register, two's complement
A8	CHGN[6]	16	0x0000	Current6Channel gain adjustment register, two's complement
A9	reserve			
AA	CHGN[V]	16	0x0000	Voltage channel gain adjustment register, two's complement
AB	reserve			

AC	CHOS[1]	16	0x0000	Current1Channel offset adjustment register, two's complement
AD	CHOS[2]	16	0x0000	Current2Channel offset adjustment register, two's complement
AE	CHOS[3]	16	0x0000	Current3Channel offset adjustment register, two's complement
AF	CHOS[4]	16	0x0000	Current4Channel offset adjustment register, two's complement
B0	reserve			
B1	reserve			
B2	CHOS[5]	16	0x0000	Current5Channel offset adjustment register, two's complement
B3	CHOS[6]	16	0x0000	Current6Channel offset adjustment register, two's complement
B4	reserve			
B5	CHOS[V]	16	0x0000	Voltage channel offset adjustment register, two's complement
B6	reserve			
B7	WATTGN[1]	16	0x0000	aisle1Active power gain adjustment register, two's complement
B8	WATTGN[2]	16	0x0000	aisle2Active power gain adjustment register, two's complement
B9	WATTGN[3]	16	0x0000	aisle3Active power gain adjustment register, two's complement
BA	WATTGN[4]	16	0x0000	aisle4Active power gain adjustment register, two's complement
BB	reserve			
BC	reserve			
BD	WATTGN[5]	16	0x0000	aisle5Active power gain adjustment register, two's complement
BE	WATTGN[6]	16	0x0000	aisle6Active power gain adjustment register, two's complement
BF	reserve			
C0	reserve			
C1	WATTOS[1]	16	0x0000	aisle1Active power bias adjustment register, two's complement
C2	WATTOS[2]	16	0x0000	aisle2Active power bias adjustment register, two's complement
C3	WATTOS[3]	16	0x0000	aisle3Active power bias adjustment register, two's complement
C4	WATTOS[4]	16	0x0000	aisle4Active power bias adjustment register, two's complement
C5	reserve			
C6	reserve			
C7	WATTOS[5]	16	0x0000	aisle5Active power bias adjustment register, two's complement

C8	WATTOS[9]	16	0x0000	Corresponding channel active power bias adjustment register, complement code
C9	reserve			
CA	VARGN	16	0x0000	Corresponding channel reactive power gain adjustment register, complement code
CB	VAROS	16	0x0000	Corresponding channel reactive power bias adjustment register, complement code
CC	VAGN	16	0x0000	Corresponding channel apparent power gain adjustment register, complement code
CD	VAOS	16	0x0000	Corresponding channel apparent power bias adjustment register, complement code
CE	CFDIV	12	0x010	CFScaling register
CF	reserve			
D0	OTP checksum	16	0x00	OTPRegister checksum,checksumIf there is a problem, restore to0 rightrega0arriveregd0

4.4Mode Register Detailed Description

4.4.1Mode Register1（MODE1）

0x96	MODE1	Working Mode Register	
No.	name	default value	description
[10:0]	WAVE_SEL	11{1'b0}	WATTFull wave waveform selection,0-AC full wave,1-DC [1]: Current1aisle;[2]: Current2aisle; [3]: Current3aisle;[4]: Current4aisle; [7]: Current5aisle;[8]: Current6aisle; [10]: Voltage channel
[21:11]	reserve		
[twenty two]	L_F_SEL	1'b0	Fast RMS selection via high pass, default is0-No Qualcomm, 1-Choose Qualcomm
[twenty three]	WAVE_REG_SEL	1'b0	CurrentWAVEWaveform register output selection, default0Select the waveform of the normal current channel,1Select fast RMS waveform input out

4.4.2Mode Register2（MODE2）

0x97	MODE2	Working Mode Register

No.	name	default value	description
[21:0]	WAVE_RMS_SEL	11{2'b00}	Effective value waveform selection: 00-AC full wave,10-DC,01-Fundamental wave,11-Full Wave [3:2]: Current1aisle;[5:4]: Current2aisle; [7:6]: Current3aisle;[9:8]: Current4aisle; [15:14]: Current5aisle;[17:16]: Current6aisle; [21:20]: Voltage channel
[twenty two]	RMS_UPDATE_SEL	1'b0	Effective value & power register update speed selection,1-105ms,0-525ms, the default selection525ms
[twenty three]	AC_FREQ_SEL	1'b0	AC frequency selection: 1-60Hz;0-50Hz, the default selection50Hz

4.4.3Mode Register3（MODE3）

0x98	MODE3	Working Mode Register	
No.	name	default value	description
[3:0]	VAR_I_SEL	4'b000	Select the reactive current measurement channel,6select1,default0000 0001-aisle1;0010-aisle2;0011-aisle3; 0100-aisle4;0111-aisle5;1000-aisle6.
[8]	add_sel	1'b0	WattThe sum of the sum of the phases is:0-Absolute value addition;1-Algebra and addition.
[9]	cf_enable	1'b0	0-cf disable,default;1-cf enable
[13:10]	CF_SEL	4'b0000	aisleCF_WATTOutput selection: 0000,1110,1111-Default offCF; 0010-aisle1PowerCF;0011-aisle2PowerCF; 0100-aisle3PowerCF;0101-aisle4PowerCF; 1000-aisle5PowerCF;1001-aisle6PowerCF; 1011-Total active powerCF; 1100-Reactive powerCF(channel optional); 1101-Apparent powerCF(channel optional); Other,CF_VARReactive powerCF(Channel optional) unchanged
[14]	hpf_sel	1'b0	hpfchoose:0-usehpf;1-Need nothpf
[15]	cf_add_sel	1'b0	WattandvarEnergy adding method: 0-Absolute value addition;1-Algebraic Sum and Addition (Partitions and Conjunctions)

[16]	var_sel	1'b0	varEnergy options:0-Fundamental wave;1-Full Wave

4.4.4Interrupt Status Register

4.4.4.1 STATUS1register

reg54	STATUS1		
Location	Interrupt flag	default value	describe
0	sag	0	Line voltage drop
1	zxto	0	Zero crossing limit
2	reserve		
3	zx01	0	Current1Channel zero crossing signal
4	zx02	0	Current2Channel zero crossing signal
5	zx03	0	Current3Channel zero crossing signal
6	zx04	0	Current4Channel zero crossing signal
7	reserve		
8	reserve		
9	zx05	0	Current5Channel zero crossing signal
10	zx06	0	Current6Channel zero crossing signal
11	reserve		
12	zx	0	Voltage channel zero crossing signal
13	reserve		
14	pk01	0	Current1Channel peak value exceeding limit signal
15	pk02	0	Current2Channel peak value exceeding limit signal
16	pk03	0	Current3Channel peak value exceeding limit signal
17	pk04	0	Current4Channel peak value exceeding limit signal
18	reserve		
19	reserve		
20	pk05	0	Current5Channel peak value exceeding limit signal

twenty one	pk06	0	Current6Channel peak value exceeding limit signal
twenty two	reserve		
twenty three	pkv		Voltage channel peak value exceeding limit signal

4.4.4.2 STATUS3register

reg56	STATUS3		
Location	Interrupt flag	default value	describe
0	reserve		
1	flag01	0	Current1Channel sign
2	flag02	0	Current2Channel sign
3	flag03	0	Current3Channel sign
4	flag04	0	Current4Channel sign
5	reserve		
6	reserve		
7	flag05	0	Current5Channel sign
8	flag06	0	Current6Channel sign
9	reserve		

M[x]Pin status;

4.5Detailed description of calibration registers

4.5.1aislePGAGain Adjust Register

7ChannelPGAGain adjustable, channelPGAGain Adjust RegisterGAIN1andGAIN2The data format is as follows:4Bit controls one channel,0000=1;0001=2;0010=8;0011=16） . Please note that the corresponding channel

After setting the gain, the maximum allowable input signal of the channel must also be reduced accordingly!

address	name	Bit width	default value	describe
60	GAIN1	twenty four	0x000000	aislePGAGain Adjust Register [3:0]: voltage channel; [11:8]:1aisle [15:12]:2aisle;[19:16]:3aisle [23:20]:4aisle

61	GAIN2	20	0x00000	aislePGAGain Adjust Register [11:8]:5aisle;[15:12]:6aisle

4.5.2Phase Correction Register

7Channel phase compensation adjustable, phase calibration registerPHASE[N]The data format is as follows:8bit to calibrate one channel, [7]reserve,[6:0]Minimum adjustment delay time250ns,correspond0.0045Spend/1LSB, the corresponding error ≈ 1.732*Sin(0.0045°)=0.0136%, maximum adjustable ±0.574The maximum adjustment error is about1.734%.

address	name	Bit width	default value	describe
64	NA/PHASE[1]	16	0x1010	[15:8]:reserve;[7:0]:1aisle
65	PHASE[2]/PHASE[3]	16	0x1010	[15:8]:2aisle;[7:0]:3aisle
66	PHASE[4]/NA	16	0x1010	[15:8]:4aisle;[7:0]:reserve
67	NA/PHASE[5]	16	0x1010	[15:8]:reserve;[7:0]:5aisle
68	PHASE[6]/NA	16	0x1010	[15:8]:6aisle;[7:0]:reserve
69	PHASE[V]	8	0x10	Voltage Channel

Adjustable phase compensation of current and voltage channels for reactive power calculation, phase calibration registerVAR_PHCAL_Iand VAR_PHCAL_VThe data format is as follows, reactive phase correction (fine tuning): [3:0]For fine-tuning,3]To enable the bit, the minimum adjustment delay time500ns,correspond0.009Spend/1LSB, , the corresponding error ≈0.0245%. Maximum adjustable ±0.072Spend.

address	name	Bit width	default value	describe
6A	VAR_PHCAL_I	4	0x0	Current channel reactive phase correction
6B	VAR_PHCAL_V	4	0x0	Voltage channel reactive phase correction

4.5.3RMS Gain Adjust Register

address	name	Bit width	default value	describe
6D	RMSGN[1]	16	0x0000	1Channel RMS gain adjustment register
6E	RMSGN[2]	16	0x0000	2Channel RMS gain adjustment register
6F	RMSGN[3]	16	0x0000	3Channel RMS gain adjustment register
70	RMSGN[4]	16	0x0000	4Channel RMS gain adjustment register
73	RMSGN[5]	16	0x0000	5Channel RMS gain adjustment register

74	RMSGN[6]	16	0x0000	6Channel RMS gain adjustment register
76	RMSGN[V]	16	0x0000	Voltage channel RMS gain adjustment register

Channel RMS gain adjustment register,16Bit complement, the highest bit is the sign bit, used for gain correction of effective value, adjustment range ±50%

$$[\ ]\_ = [\ ]\_0 * (1 + \frac{[\ ]}{2^{16}})$$

inI[N]_RMS0For theNThe measured value of the channel,RMSGN[N]is the gain correction value,I[N]_RMSis the corresponding calibration output value.

4.5.4RMS offset correction register

address	name	Bit width	default value	describe
78	RMSOS[1]	twenty four	0x000000	1Channel RMS offset correction register
79	RMSOS[2]	twenty four	0x000000	2Channel RMS offset correction register
7A	RMSOS[3]	twenty four	0x000000	3Channel RMS offset correction register
7B	RMSOS[4]	twenty four	0x000000	4Channel RMS offset correction register
7E	RMSOS[5]	twenty four	0x000000	5Channel RMS offset correction register
7F	RMSOS[6]	twenty four	0x000000	6Channel RMS offset correction register
81	RMSOS[V]	twenty four	0x000000	Voltage channel RMS offset correction register

Channel RMS offset correction register,twenty fourBit complement, the highest bit is the sign bit. It is used to eliminate the deviation caused by input noise in the effective value calculation, so that the effective value register value is close to0.

$$[\ ]\_ = \sqrt{[\ ]\_0{}^2 + [\ ] * 256}$$

inI[N]_RMS0For theNThe measured value of the channel,RMSOS[N]is the bias correction value,I[N]_RMSis the corresponding calibration output value.

4.5.5Active small signal compensation register

address	name	Bit width	default value	describe
82	NA/ WA_LOS[1]	twenty four	0x000000	[23:12]:reserve [11:0]:aisle1Active power small signal compensation register
83	WA_LOS[2]/	twenty four	0x000000	[23:12]:aisle2Active power small signal compensation register

	WA_LOS[3]			[11:0]:aisle3Active power small signal compensation register
84	WA_LOS[4]/ NA	twenty four	0x000000	[23:12]:aisle4Active power small signal compensation register [11:0]:reserve
85	NA/ WA_LOS[5]	twenty four	0x000000	[23:12]:reserve [11:0]:aisle5Active power small signal compensation register
86	WA_LOS[6]/ NA	twenty four	0x000000	[23:12]:aisle6Active power small signal compensation register [11:0]:reserve

The active power small signal compensation register is used to compensate for the active small signal deviation caused by DC bias.

$$[\ ] = \quad 0[\ ] + \ \_ \ [\ ] * 2$$

inWATT0[N]For theNThe measured value of the channel,WA_LOS[N]is the bias correction value,WATT[N]is the calibration output value of the corresponding channel.

NoticeWA_LOS[N]It is a signed number, complement code, which can correct the active power register within the range of ±4094.

4.5.6Reactive small signal compensation register

address	name	Bit width	default value	describe
87	FVAR_LOS/VAR_LOS	twenty four	0x000000	[11:0]Corresponding to the reactive (full wave) small signal compensation register, code. [23:12]Corresponding to the reactive (fundamental) small signal compensation register, code.

VAR_LOSformula:

$$= \quad 0 + \ \_ \ * 2$$

inVAR0is the measured value of reactive power,VAR_LOSis the bias correction value,VARis the calibration output value.

NoticeVAR_LOSIt is a signed number, two's complement, which can correct the reactive power register within the range of ±4094.

FVAR_LOSThe formula is similar.

4.5.7Anti-creep Threshold Register

address	name	Bit width	default value	describe
88	VAR_CREEP/ WA_CREEP	twenty four	0x04C04C	[11:0]Active anti-creep power threshold registerWA_CREEP; [23:12] Reactive power protection threshold registerVAR_CREEP;
89	WA_CREEP2	12	0x000	[11:0]Total active power anti-creep threshold register

The anti-creep power threshold register is used to set the active power/reactive power anti-creep of each channel. When a channel is in the anti-creep state, the power below the threshold of the channel will not be included in the energy accumulation.

When the absolute value of the input power signal is less than this value, the output power register value is set to zero. This allows the value output to the active power register to be zero even with a small noise signal in the no-load condition.0.

$$\text{correspond} \quad \text{Value} = \frac{\text{Corresponding power register value}}{2}$$

6The anti-creep threshold setting of the total active power of the circuit.Reg88Register, this register can be set Set.

$$\_ \quad 2 = \frac{\text{Register Value}}{2}$$

address	name	Bit width	default value	describe
8A	RMS_CREEP	12	0x200	RMS small signal threshold register

It can make the value output to the effective value register be0.

$$\_ \quad = [\,]\_$$

4.5.8Fast effective value related setting register

address	name	Bit width	default value	describe
8B	FAST_RMS_CTRL	twenty four	0x20FFFF	[23:21]Channel fast effective value register refresh time, optional half cycle Wave andNFrequency, the default is frequency; [20:0]Channel Fast RMS Threshold Register

Depend onFAST_RMS_CTRL[23:21]Select the cumulative time, minutes10ms（000） ,20ms（001）、40ms（010）,80ms（011）,160ms（100）,320ms（101) There are six types, the default is (001) Select frequency accumulation response Response time20msThe longer the accumulated time, the smaller the jump.

FAST_RMS_CTRL[20:0]Used to set the fast effective value exceeding the limit threshold. Once exceeded, the output flagflag[N] for1. Flag bit connection output (M1~M6), you can directly pull the leakage/overcurrent output indication pin high. It can be used in conjunction with the overcurrent indication control register.

$$\_ \quad \_ \quad [20:0] = \frac{[\,]\_ \quad \_}{8}$$

4.5.9Overcurrent alarm and control

address	name	Bit width	default value	describe

90	flag_ctrl	twenty four	0x000000	Master direct controlM6~M1Output level status [20:13]:M6~M1Output priority [8:1]:M6~M1Pin output level [1]:1aisle;[13]; [2]:2aisle;[14] [3]:3aisle;[15] [4]:4aisle;[16] [7]:5aisle;[19] [8]:6aisle;[20]
91	flag_ctrl1	twenty four	0x000000	Overcurrent indication control register1. [23:10]: Disconnect delay timer,0.1ms/lsb; [9:0]Indicator control,M1-M6:0-Output real-time interrupt;1-Output delay control [1]:1aisle;[2]:2aisle; [3]:3aisle;[4]:4aisle; [7]:5aisle;[8]:6aisle;
92	flag_ctrl2	twenty four	0x000000	Overcurrent indication control register2. [23:10]: Closing delay timing,0.1ms/lsb; [9:0]Closed control,M1-M6:0-closure,1-disconnect [1]:1aisle;[2]:2aisle; [3]:3aisle;[4]:4aisle; [7]:5aisle;[8]:6aisle;

flag_ctrlregister,Bit[8:1]forM6~M1Output level control;

Bit[20:13]forM6~M1The control priority of the output, the corresponding position is1WhenBit[9:0]The corresponding bit state directly controlsM6~M1Output level.flag_ctrl1, flag_ctrl2has a higher priority.

Real-time alarm output

passM6~M1The pin outputs the alarm high level of the corresponding channel in real time. Only the overcurrent (leakage) threshold register is set Reg8B（FAST_RMS_CTRL), fast effective value refresh time/fast effective value threshold;

Delay control logic description

set upReg8BRegister, fast RMS refresh time/fast RMS threshold;

set upReg91register,Bit[23:10]Delay output high level timeT1,Bit[9:0]Turn on the delay control of the corresponding channel;

set upReg92register,Bit[23:10]Delay output low level timeT2,Bit[9:0]=0;

---------- Running the process ----------

If the channelNAfter a fast RMS value exceeding limit event occursI[N]_FAST_RMS_HOLDThe register retains the quick valid value when the limit is exceeded; thenT1Seconds, corresponding toM[N]Pull the pin high.Reg56The corresponding indication status bits of the register are1;

---------- After the rapid effective value exceeds the limit fault is eliminated----------

MCUTowardsReg92Register write delay output low level timeT2,Bit[9:0]The corresponding channel [N]Location is1; M[N]Pin DelayT2After a certain time,Reg56Status cleared;

MCUTowardsReg92Register write,Bit[23:10]=T2Delay time,Bit[9:0]The corresponding channel [N]Location is 0, clear the correspondingI[N]_FAST_RMSHOLDRegister value.

4.5.10 ADCEnable control

address	name	Bit width	default value	describe
93	ADC_PD	11	0x000	7ChannelsADCEnable control: [0]-Voltage channel; [2]-1aisle; [3]-2aisle;[4]-3aisle; [5]-4aisle;[8]-5aisle; [9]-6aisle;

Power consumption can be reduced by shutting down unused channels.Bit[10:0]Corresponding position1, close the corresponding channel ADC. Unused bits [1]、[6:7]、[10]Set to1.

4.5.11Energy read clear setting register

address	name	Bit width	default value	describe
9D	RST_ENG	13	0x0000	Energy pulse counting register clear after reading

Bit[12:0]Set to1When the power related registersReg3B~2FSet to clear after reading. Can be set individually.

Bit	12	11	. . .	2	1	0
Energy pulse register value address (0x)	3B	3A	. . .	31	30	2F

4.5.12User write protection setting register

address	name	Bit width	default value	describe
9E	USR_WRPROT	16	0x0000	User write protection setting register, write0x5555When , it indicates that the user register pair can be operatedreg60arrivereg9d,rega0arrived0

BL0906There is a strict protection mechanism for register writing, and you must first write to the write protection setting register 0x5555, before writing to other registers.

4.5.13Soft reset register

address	name	Bit width	default value	describe
9F	SOFT_RESET	twenty four	0x000000	When the input is5A5A5AWhen the system is reset, only the digital part is reset. The state machine and registers (0x01~0x5F)! When the input is55AA55When the user reads and writes the registers, they are reset. Reset:reg60arrivereg9f,rega0arriveregd0

4.5.14Channel gain adjustment register

address	name	Bit width	default value	describe
A1	CHGN[1]	16	0x0000	1Channel channel gain adjustment register, two's complement
A2	CHGN[2]	16	0x0000	2Channel channel gain adjustment register, two's complement
A3	CHGN[3]	16	0x0000	3Channel channel gain adjustment register, two's complement
A4	CHGN[4]	16	0x0000	4Channel channel gain adjustment register, two's complement
A7	CHGN[5]	16	0x0000	5Channel channel gain adjustment register, two's complement
A8	CHGN[6]	16	0x0000	6Channel channel gain adjustment register, two's complement
AA	CHGN[7]	16	0x0000	Voltage channel gain adjustment register, two's complement

Channel gain adjustment register,16bit signed number,2The complement form adjusts the corresponding channelADThe gain of the sampling waveform can be adjusted within the range of ±50%

$$[\ ] = \quad 0[\ ] * (1 + \frac{[\ ]}{2^{16}})$$

inWAVE0[N]For theNThe measured value of the channel,CHGN[N]is the gain calibration value,WAVE[N]For calibration output value.

4.5.15Channel offset adjustment register

address	name	Bit width	default value	describe
AC	CHOS[1]	16	0x0000	1Channel offset adjustment register, two's complement
AD	CHOS[2]	16	0x0000	2Channel offset adjustment register, two's complement
AE	CHOS[3]	16	0x0000	3Channel offset adjustment register, two's complement

AF	CHOS[4]	16	0x0000	4Channel offset adjustment register, two's complement
B2	CHOS[5]	16	0x0000	5Channel offset adjustment register, two's complement
B3	CHOS[6]	16	0x0000	6Channel offset adjustment register, two's complement
B5	CHOS[7]	16	0x0000	7Channel offset adjustment register, two's complement

Channel offset adjustment register to2The data in the form of two's complement is used to eliminate the deviation caused by the analog-to-digital conversion of the current channel and the voltage channel. The deviation here may be caused by the input and the analog-to-digital conversion circuit itself.offsetDeviation correction can make the waveform in no-load conditionoffsetfor0.

$$WAVE[N] = WAVE0[N] + CHOS[N]$$

inWAVE0[N]For theNThe measured value of the channel,CHOS[N]is the calibration value,WAVE[N]The output after calibration value.

4.5.16Active power gain adjustment register

address	name	Bit width	default value	describe
B7	WATTGN[1]	16	0x0000	aisle1Active power gain adjustment register, two's complement
B8	WATTGN[2]	16	0x0000	aisle2Active power gain adjustment register, two's complement
B9	WATTGN[3]	16	0x0000	aisle3Active power gain adjustment register, two's complement
BA	WATTGN[4]	16	0x0000	aisle4Active power gain adjustment register, two's complement
BD	WATTGN[5]	16	0x0000	aisle5Active power gain adjustment register, two's complement
BE	WATTGN[6]	16	0x0000	aisle6Active power gain adjustment register, two's complement

Active power gain adjustment register,16bit signed number,2The complement form adjusts the corresponding channel power gain:

$$WATT[N] = WATT0[N] * (1 + \frac{[\,]}{2^{16}})$$

inWATT[N]It isNThe active power after the road correction,WATT0[N]It isNActive power before circuit correction. Adjustment range ±50%.

4.5.17Active power bias adjustment register

address	name	Bit width	default value	describe
C1	WATTOS[1]	16	0x0000	aisle1Active power bias adjustment register, two's complement
C2	WATTOS[2]	16	0x0000	aisle2Active power bias adjustment register, two's complement

C3	WATTOS[3]	16	0x0000	aisle3Active power bias adjustment register, two's complement
C4	WATTOS[4]	16	0x0000	aisle4Active power bias adjustment register, two's complement
C7	WATTOS[5]	16	0x0000	aisle5Active power bias adjustment register, two's complement
C8	WATTOS[6]	16	0x0000	aisle6Active power bias adjustment register, two's complement

Active power bias adjustment register, two's complement, highest bit is the sign bit. Used to eliminate active power deviation caused by board-level noise.

$$[\,] = 0[\,] + \frac{[\,]}{2}$$

inWATT0[N]For theNThe measured value of the channel,WATTOS[N]is the bias correction value,WATT[N]is the corresponding calibration output value.

4.5.18Reactive/apparent power gain adjustment register

address	name	Bit width	default value	describe
CA	VARGN	16	0x0000	Corresponding channel reactive power gain adjustment register, complement code
CC	VAGN	16	0x0000	Corresponding channel apparent power bias adjustment register, complement code

The adjustment formula is similar to the active power gain adjustment.

4.5.19Reactive/apparent power bias adjustment register

address	name	Bit width	default value	describe
CB	VAROS	16	0x0000	Corresponding channel reactive power bias adjustment register, complement code
CD	VAOS	16	0x0000	Corresponding channel apparent power bias adjustment register, complement code

The adjustment formula is similar to the active power bias adjustment.

4.5.20 CFScaling register

Used to control the accumulation speed of electric energy pulse counting.BL0906The default setting is0x10.

address	name	Bit width	default value	describe
CE	CFDIV	12	0x010	CFScaling register

byCFDIV=0x10The frequency of the energy pulse count is used as the standard frequency, and the multiples of the energy pulse count for other settings are as follows:

CFDIV	Counting rate
0x00	0.03125
0x01	0.0625
0x02	0.125
0x04	0.25
0x08	0.5
0x10	1
0x20	2
0x40	4
0x80	8
0x100	16
0x200	32
0x400	64
0x800	256
Other Values	1

4.6Detailed description of electrical parameter registers

4.6.1Waveform register

address	name	Bit width	default value	describe
2	I[1]_WAVE	twenty four	0x000000	1Channel waveform register (normal current and fast current optional)
3	I[2]_WAVE	twenty four	0x000000	2Channel waveform register (normal current and fast current optional)
4	I[3]_WAVE	twenty four	0x000000	3Channel waveform register (normal current and fast current optional)
5	I[4]_WAVE	twenty four	0x000000	4Channel waveform register (normal current and fast current optional)
8	I[5]_WAVE	twenty four	0x000000	5Channel waveform register (normal current and fast current optional)
9	I[6]_WAVE	twenty four	0x000000	6Channel waveform register (normal current and fast current optional)
B	V_WAVE	twenty four	0x000000	Voltage channel waveform register

Waveform data of real-time sampling points, sampling clock4MHz,4MHz/256/50=312.5, each cycle is about312sampling points.

4.6.2Effective value register

address	name	Bit width	default value	describe
D	I[1]_RMS	twenty four	0x000000	1Channel RMS register
E	I[2]_RMS	twenty four	0x000000	2Channel RMS register
F	I[3]_RMS	twenty four	0x000000	3Channel RMS register
10	I[4]_RMS	twenty four	0x000000	4Channel RMS register
13	I[5]_RMS	twenty four	0x000000	5Channel RMS register
14	I[6]_RMS	twenty four	0x000000	6Channel RMS register
16	V_RMS	twenty four	0x000000	Voltage channel effective value register

Can be setMODE2[22]ofRMS_UPDATE_SEL,The selectable effective value average refresh time is525ms or1.05s,default525ms.

4.6.3Fast RMS Register

address	name	Bit width	default value	describe
18	I[1]_FAST_RMS	twenty four	0x000000	1Channel fast RMS register
19	I[2]_FAST_RMS	twenty four	0x000000	2Channel fast RMS register
1A	I[3]_FAST_RMS	twenty four	0x000000	3Channel fast RMS register
1B	I[4]_FAST_RMS	twenty four	0x000000	4Channel fast RMS register
1E	I[5]_FAST_RMS	twenty four	0x000000	5Channel fast RMS register
1F	I[6]_FAST_RMS	twenty four	0x000000	6Channel fast RMS register
twenty one	V_FAST_RMS	twenty four	0x000000	Voltage channel fast RMS register

For over-current or leakage detection, the detection cycle can beFAST_RMS_CTRLRegister settings. Note that the smaller the detection period, the greater the fluctuation of the register value.

$$[\,]\_\ \_\ \approx [\,]\_\ * 0.55$$

4.6.4Active Power Register

address	name	Bit width	default value	describe
twenty three	WATT[1]	twenty four	0x000000	aisle1Active Power Register
twenty four	WATT[2]	twenty four	0x000000	aisle2Active Power Register
25	WATT[3]	twenty four	0x000000	aisle3Active Power Register
26	WATT[4]	twenty four	0x000000	aisle4Active Power Register
29	WATT[5]	twenty four	0x000000	aisle5Active Power Register
2A	WATT[6]	twenty four	0x000000	aisle6Active Power Register
2C	WATT	twenty four	0x000000	Total active power register

The active power register is signedtwenty fourbit data, complement code. The highest bit is the sign bit,Bit[23]=1,Indicates that the current power is negative;

$$= \frac{(\quad [\,])}{16}$$

4.6.5Reactive power register

address	name	Bit width	default value	describe
2D	FVAR	twenty four	0x000000	Optional channel reactive power register (fundamental)
5D	VAR	twenty four	0x000000	Optional channel reactive power register (full wave)

Signedtwenty fourBit data, complement.Bit[23]is the sign bit,1Indicates that the current power is negative;MODE3[3:0]Used to select the reactive power measurement channel.

4.6.6Apparent Power Register

address	name	Bit width	default value	describe
2E	VA	twenty four	0x000000	Selectable channel apparent power register

4.6.7Energy pulse counting register

address	name	Bit width	default value	describe
30	CF[1]_CNT	twenty four	0x000000	aisle1Active pulse count, unsigned
31	CF[2]_CNT	twenty four	0x000000	aisle2Active pulse count, unsigned
32	CF[3]_CNT	twenty four	0x000000	aisle3Active pulse count, unsigned
33	CF[4]_CNT	twenty four	0x000000	aisle4Active pulse count, unsigned
36	CF[5]_CNT	twenty four	0x000000	aisle5Active pulse count, unsigned
37	CF[6]_CNT	twenty four	0x000000	aisle6Active pulse count, unsigned
39	CF_CNT	twenty four	0x000000	Total active pulse count, unsigned
3A	CFQ_CNT	twenty four	0x000000	Optional channel reactive pulse count, unsigned
3B	CFS_CNT	twenty four	0x000000	Selectable channel apparent pulse count, unsigned

Energy pulse counting, andCFDIVRegister related,CFDIVThe larger the register setting value, the faster the pulse count.

MODE3[15]Used to set the energy pulse counting accumulation mode: algebraic sum/absolute value mode;

RST_ENGThe register is used to set whether the energy pulse counting register is cleared after reading;

$$- = \frac{([ ])}{16}$$

4.6.8Waveform Angle Register

address	name	Bit width	default value	describe
3D	ANGLE[1]	16	0x0000	aisle1Current and voltage waveform angle register
3E	ANGLE[2]	16	0x0000	aisle2Current and voltage waveform angle register
3F	ANGLE[3]	16	0x0000	aisle3Current and voltage waveform angle register
40	ANGLE[4]	16	0x0000	aisle4Current and voltage waveform angle register
43	ANGLE[5]	16	0x0000	aisle5Current and voltage waveform angle register
44	ANGLE[6]	16	0x0000	aisle6Current and voltage waveform angle register

It should be noted that when the current is less than a certain value, the angle register stops working.

$$\text{Angle (°)} = \frac{360 * [ ] *}{500000}$$

fcis the measurement frequency of the AC signal source, the default is50Hz

Fast RMS Holding Register

address	name	Bit width	default value	describe
47	I[1]_FAST_RMS_H	twenty four	0x000000	1Channel fast effective value storage register
48	I[2]_FAST_RMS_H	twenty four	0x000000	2Channel fast effective value storage register
49	I[3]_FAST_RMS_H	twenty four	0x000000	3Channel fast effective value storage register
57	I[4]_FAST_RMS_H	twenty four	0x000000	4Channel fast effective value storage register
5A	I[5]_FAST_RMS_H	twenty four	0x000000	5Channel fast effective value storage register
5B	I[6]_FAST_RMS_H	twenty four	0x000000	6Channel fast effective value storage register

Data exceeding the fast effective value threshold is stored in the correspondingI[x]_FAST_RMS_HOLDIn the register, it needs to be cleared through a set operation.

1）flag_ctrl2[9:0]The corresponding bit is set to1;

2）flag_ctrl2[9:0]The corresponding bit is set to0; Clear the correspondingFAST_RMS_HOLDRegister value;

4.6.9Power Factor Register

address	name	Bit width	default value	describe
4A	PF	twenty four	0x000000	Selectable channel power factor register

Depend onVAR_I_SELRegister selection, that is, which channel is selected for reactive power and which channel is also selected for power factor.

twenty fourBit signed number, two's complement.Bit[23]is the sign bit,

$$\text{Power Factor} = \frac{\quad}{2^{\text{twenty three}}}$$

4.6.10Line voltage frequency period register

address	name	Bit width	default value	describe
4E	PERIOD	20	0x00000	Line voltage frequency period register

Measure the frequency of the sine wave signal of the voltage channel.

Line voltage frequency = 1000000Hz

5.Communication interface

Register data are all in3byte(24bit) sent, insufficient3Byte register data, bit complement not used0, make up3 Bytes sent.

Through the pinSELchoose,SEL=1The time isSPI,SEL=0The time isUART

5.1 SPI

5.1.1Overview

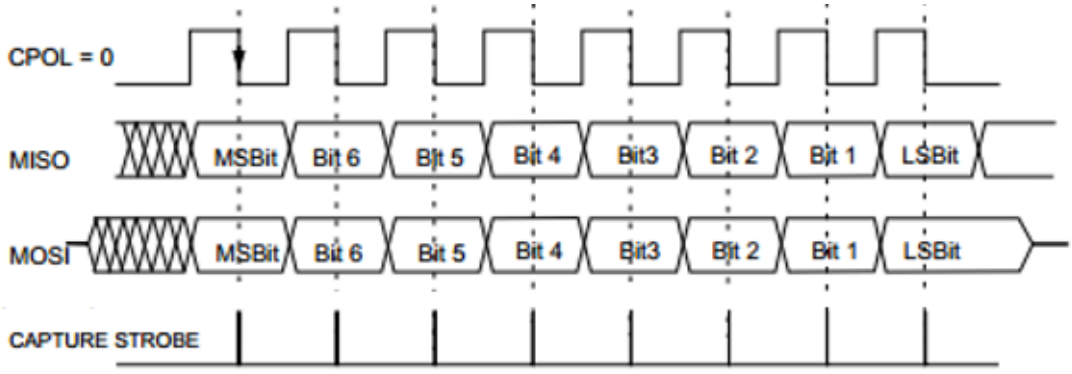
Slave mode, half-duplex communication, maximum communication rate1.5M

8-bitData transmission,MSBin front,LSBIn the back

Fixed clock polarity/phase (CPOL=0,CPHA=1）

5.1.2Working Mode

The master device works inMode1:CPOL=0,CPHA=1, that is, in idle state,SCLKAt low level, data is sent in the1 edge, that isSCLKThe jump from low level to high level, so data sampling is on the falling edge and data sending is on the rising edge.



5.1.3Frame structure

In communication mode, send first8bitIdentification Bytes (0x81)or(0x82), (0x82)is the read identification byte, (0x81)Write the identification byte and then send the register address byte to determine the address of the register to be accessed (seeBL0906 Register List). The following figure shows the data transfer sequence for read and write operations respectively.BL0906Re-enter communication mode. Each read/write operation requiresSCLKThe number of pulses is48Bit.

There are two frame structures, which are described as follows:

1）Write register

Cmd: {0x81}+ Addr+Data_H+Data_M+Data_L+SUM

{0x81}Frame identification byte for write operation;

AddrFor write operationsBL0906The internal register address of

The checksum byteCHECKSUMfor(({0x81}+ ADDR+ DATA_H+ DATA_M+ DATA_L）

& 0xFF) and then negate the bitwise value.

Write Operation Frame	0x81	ADDR[7:0]	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

2）Read register

Cmd:{0x82}+Addr

return:Data_H+Data_M+Data_L+SUM

{0x82}Frame identification byte for read operation;

AddrFor read operationsBL0906The internal register address (0x00-0xff);

The checksum byteCHECKSUMfor(({0x82}+ ADDR+ DATA_H+ DATA_M+ DATA_L）

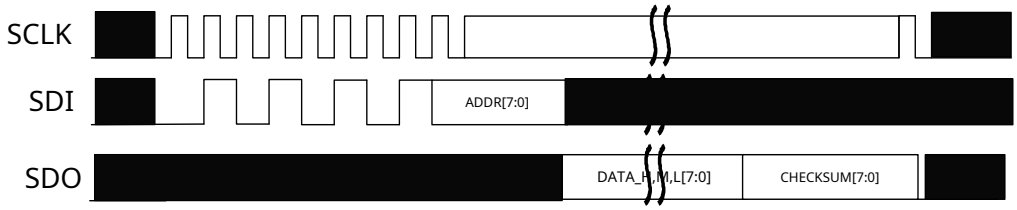
& 0xFF) and then negate the bitwise value.

Read command frame	0x82	ADDR[7:0]

Reading Data Frame	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

5.1.4Read Operation Timing

In the rightBL0906During data read operation,SCLKThe rising edge ofBL0906Move the corresponding data bit toDOUTLogic output pins, in the nextSCLKfor1within the time,DOUTThe value remains unchanged, that is, at the next falling edge, the external device canDOUTAs with the data write operation, before the data read operationMCUThe identification byte and address byte must be sent first.



whenBL0906When in communication mode, the frame identification byte {0x82}, indicating that the next data transfer operation is to read. Then the following byte is the address of the target register to be read.BL0906existSCLKThe rising edge of the OUTPUT register starts shifting out the data in the register. All remaining bits of the register data are shifted out on the following OUTPUT registers.SCLKTherefore, on the falling edge, the external device canSPIOnce the read operation is completed, the serial interface re-enters the communication mode.DOUTThe logic output is at the lastSCLKThe falling edge of the signal enters the high-impedance state.

5.1.5Write Operation Timing

The serial write sequence is as follows. Frame Identification Byte {0x81}, indicating that data is written during transfer operation.MCU Will need to writeBL0906The data bit isSCLKPrepare before the lower edge ofSCLKThe falling edge of this clock starts shifting in the register data. All remaining bits of the register data are also shifted in at thisSCLKThe falling edge of the bit is shifted left.

5.1.6 SPIFault tolerance mechanism of the interface

1) If the frame recognition byte is wrong orSUMIf a byte is wrong, the frame data is discarded.

2）SPIModule reset: BySPIInterface delivery6Bytes0xFF, can be used separatelySPIThe interface is reset;

3)_CSPull high to reset.

5.2 UART

5.2.1Overview

Through the pinUART_SELchoose,SEL=1The time isSPI,SEL=0The time isUART

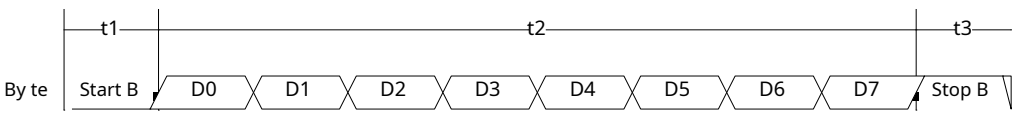
The communication baud rate is4800bps/9600bps/19200bps/38400bps/, no parity, stop bit1;

Baud rate setting	4800	9600	19200	38400
CSPins	0	0	1	1
SCLKPins	0	1	0	1

UARTMode,CS,SCLKThe pin is used as the baud rate setting pin.

5.2.2Each byte format

by4800bpsFor example:



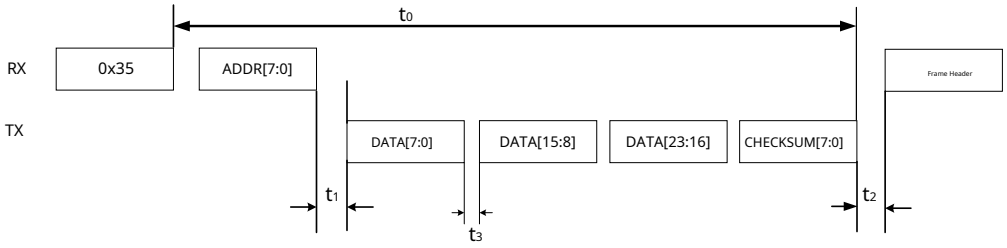
Start bit low level duration1=208us(4800bps);

Valid data bit time duration2=208*8=1664us(4800bps);

Stop bit high level durationt3=208u(4800bps)s;

5.2.3Read Timing

HostUARTThe read data timing is shown in the figure below. The host first sends the command byte (0x35), and then send the address byte to be read (ADDR） NextBL0906The data bytes are sent sequentially, followed by the checksum byte at the end.



{0x35}Frame identification byte for read operation;

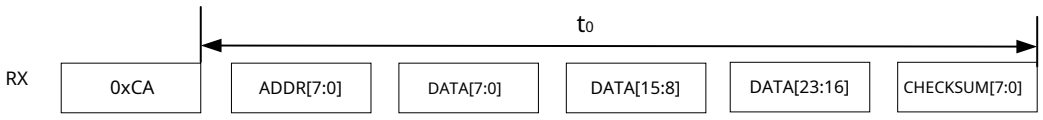
AddrFor read operationsBL0906The internal register address of

SUMBytes are (Addr+Data_L+Data_M+Data_H)&0xFFNegate;

	Read Timing Description	Min	Type	Max	Unit
t0	Frame length (excluding frame identification bytes)			16	mxD
t1	During read operationMCUSend register address end to BL0906The interval between sending bytes		120		uS
t2	Frame interval time	1t_{bit}			
t3	BL0906Returns the byte interval time		1t_{bit}		

5.2.4Write Timing

HostUARTThe data writing sequence is shown in the figure below. The host first sends the command byte (0xCA), followed by the write address byte (ADDR), followed by the data bytes and finally the checksum byte.



{0xCA}Frame identification byte for write operation;

AddrFor write operationsBL0906The internal register address of

CHECKSUMBytes are ((ADDR+Data_L+Data_M+Data_H)&0xFF) and then negate the bitwise value.

	Write Timing Description	Min	Type	Max	Unit
t0	Frame length (excluding frame identification bytes)			16	mxD

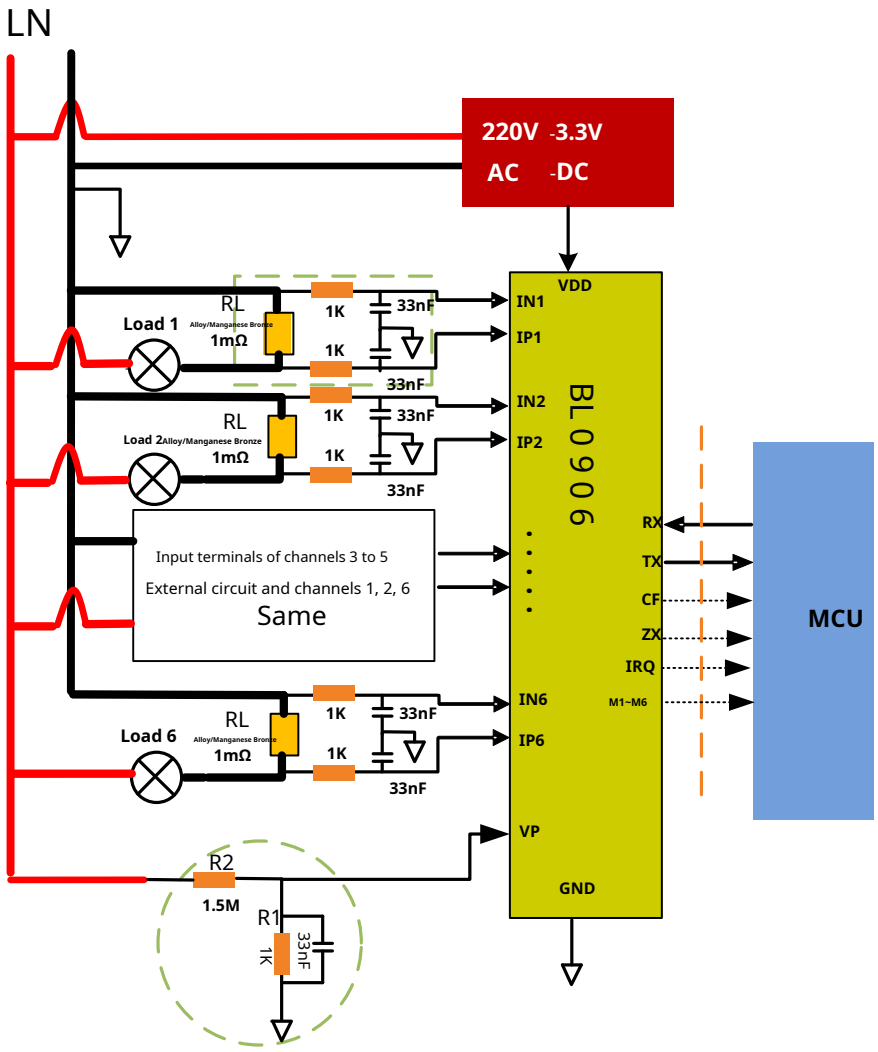
5.2.5 UARTInterface protection mechanism

BL0906ofUARTCommunication provides a timeout protection mechanism. After the frame times out,UARTInterface reset. If read operation fails, wait > 20mS, and then proceed to the next frame read and write operation.

If the frame identification byte is wrong orCHECKSUMIf a byte is wrong, the frame data is discarded.

UARTModule reset:RXThe pin low level exceeds32indivualt$_{bit}$（4800bpsTime6.67ms) and then pull high, UARTModule reset.

6.Typical application diagram



The external circuit diagram of each current channel is the same, and the voltage channel requires signal voltage division.

7.Packaging information

7.1Order Information

BL0906 LQFP32Encapsulation

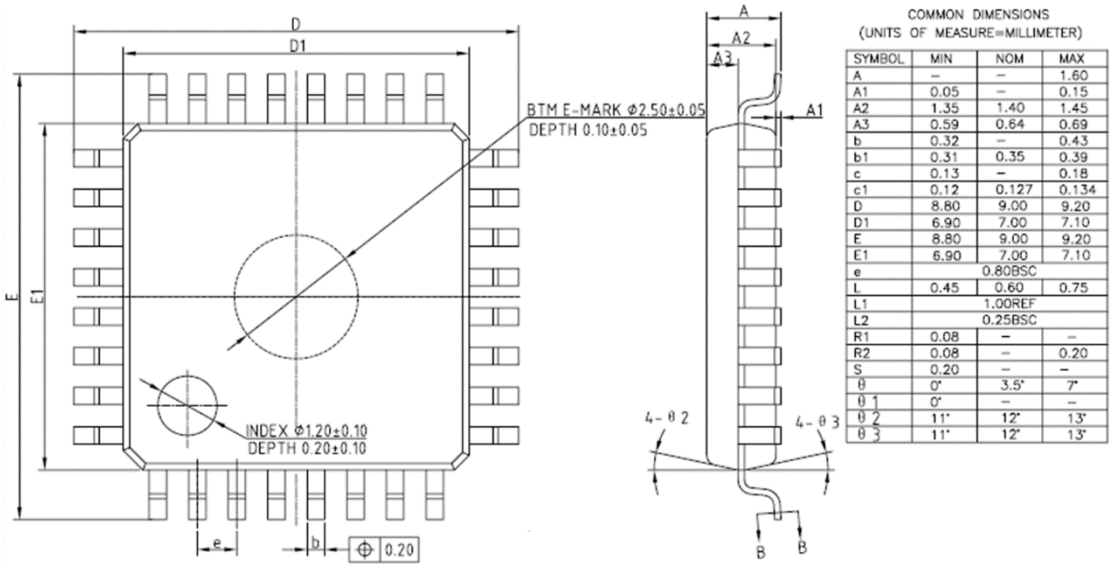
7.2Encapsulation

Moisture sensitivity level MSL 3

Two-year warranty

Packaging Tray

7.3Package appearance



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	–	0.43
b1	0.31	0.35	0.39
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.80BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

8. Version Information

Version Number	Modification time	Modifications
V1.0	2020/06/20	create
V1.01	2021/04/11	Errata Correction
V1.02	2021/11/21	Add DC description
V1.10	2024/07/19	1) UART communication timing description revised 2) Revised some functional descriptions