

### Product Description:

PL1167 is a piece of true low power high performance single chip 2.4GHz transceiver, which is designed for operation in the world wide ISM frequency band at 2.400~2.4835GHz.

This single chip wireless transceiver integrated including: RF synthesizer, Power Amplifier, Crystal Oscillator, Modem and etc.

All of the Output Power, Channel Selection, and Protocol can be configured through SPI/I2C Interface.

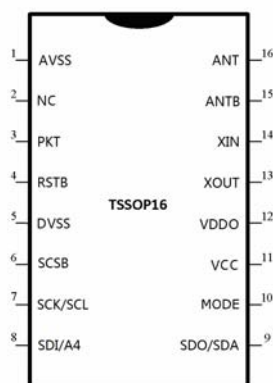
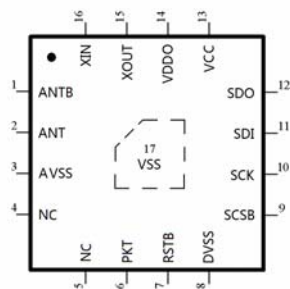
With built in FHSS and accurate digital RSSI, this transceiver achieves a good capability of anti-interference, so that, it can work under every complicated environment with high performance.

It also support address and data check out; FEC, CRC function; and Auto-Ack & Auto-Resend function.

The output power of the chip can be set up to 5.5dBm and the receive sensitivity can achieve -88dBm.

With on chip regulator and advanced power management function, the current consumption in sleep mode can be reduced to nearly 1uA.

### Pin Configuration:



### Key Features:

- True Low Power High Performance Single Chip 2.4GHz Transceiver
- Built in Hardware Link Layer
- Built in Accurate Digital RSSI
- Support Auto-Ack and Auto-Resend Functions
- Built in Address and Data Checkout, FEC, CRC Functions
- Data Rate over the air: 1Mbps
- Support HFSS
- Support Micro-Strip Inductor and Two Layer PCB Boards
- 1.9 to 3.6V supply range
- Packages: QFN16/ TSSOP16
- QFN16 only support SPI Interface
- TSSOP16 support SPI and I2C Interface

### Applications:

- Wireless Mice, keyboards and Game Controllers
- Wireless Data Communication
- Wireless Door Accessing
- Wireless Networks
- Safety and Guard System
- RF Remote Control
- Remote Sensing
- Sports watches and sensors
- Home and commercial automation
- Industrial Sensors
- Industrial and Commercial Short Range Communication
- VoIP headsets
- Toys



# 1 Overview

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# 2 Features

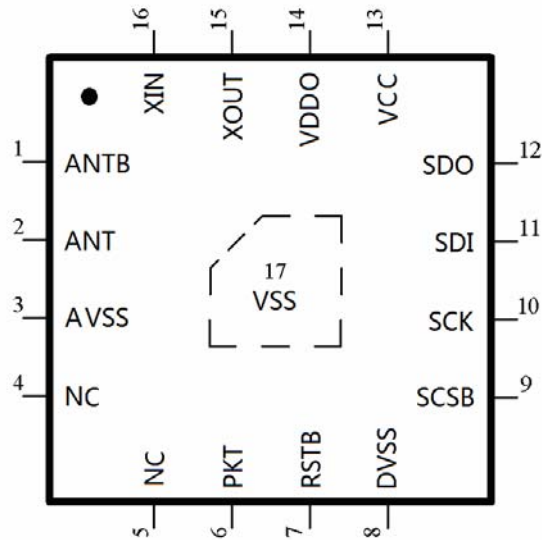
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# 3 Quick Reference Data

Parameter	Value	Units
Min Supply Voltage	1.9	V
Max Output Power	5.5	dBm
Data Rate	1	Mbps
Current Consumption (0dBm) @TX Mode	16	mA
Current Consumption @RX Mode	17	mA
Operating Temperature Range	-40 to +85	°C
RX Sensitivity	-88	dBm
Current Consumption @Sleep Mode	1	uA

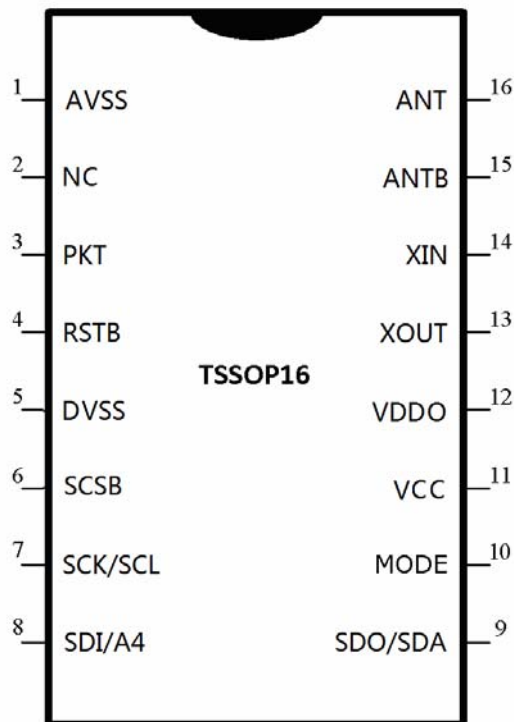
## 4 Pin Diagrams

The pin map is shown as below for QFN16.



*Note: MODE pin is connected to VSS in the chip, so QFN16 is only supported SPI interface.*

The pin map is shown as below for TSSOP16.



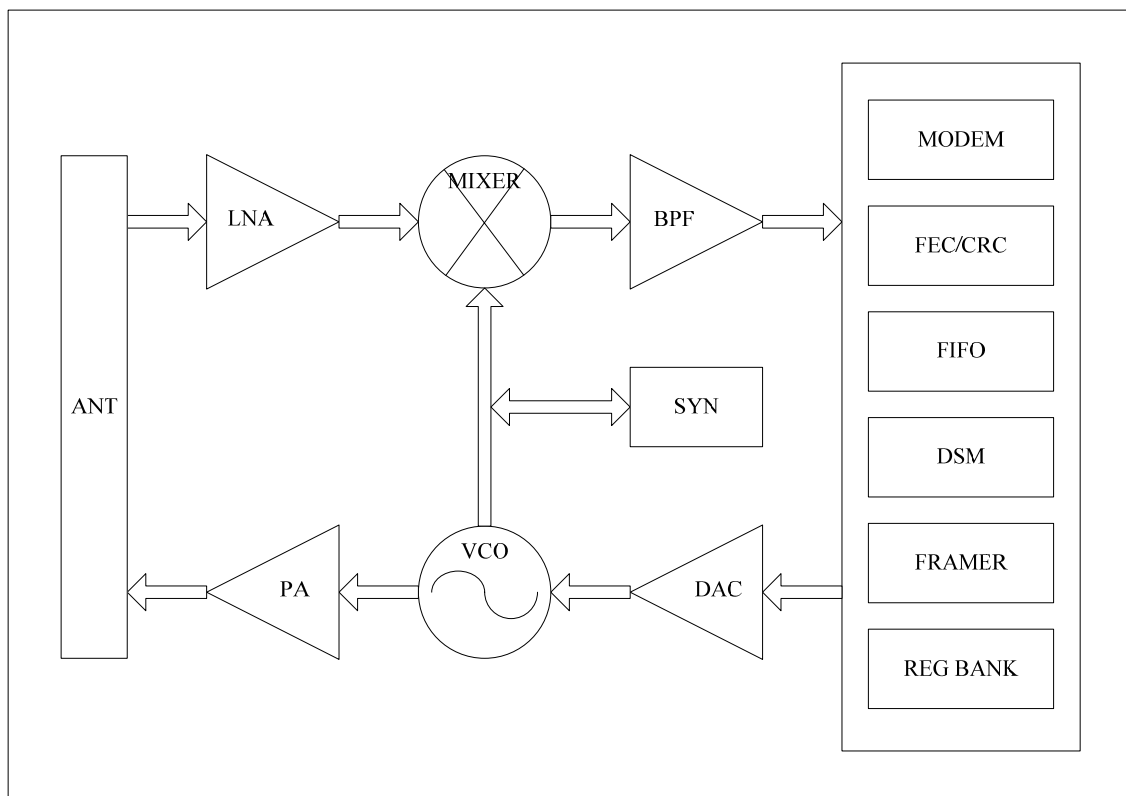
## 5 Pin Description

Pin(QFN16)	Name	Pin Function	Description
1	ANTB	RF	Antenna Interface
2	ANT	RF	Antenna Interface
3,8,17	VSS	Power	Ground (0V)
4,5	NC	N/C	Not Connected
6	PKT	Digital Output	Transmit/Receive Packet Status Indicator Bit
7	RSTB	Digital Input	Reset Pin, active low
9	SCSB	Digital Input	Enable Input for SPI Interface, active Low Wakeup from SLEEP state
10	SCK	Digital Input	Clock Input for SPI Interface
11	SDI	Digital Input	Data Input for SPI Interface
12	SDO	Digital Output	Data Output for SPI Interface (tri-state when not active)
13	VCC	Power	Power Supply (3.3V)
14	VDDO	Power	1.8V power output, connect to capacitor
15	XOUT	Analog Output	Crystal Oscillator Output
16	XIN	Analog Input	Crystal Oscillator Input

Pin(TSSOP16)	Name	Pin Function	Description
1	AVSS	Power	Ground (0V)
2	NC	N/C	Not Connected
3	PKT	Digital Output	Transmit/Receive Packet Status Indicator Bit
4	RSTB	Digital Input	Reset Pin, active low
5	DVSS	Power	Ground (0V)
6	SCSB	Digital Input	SPI: Enable Input for SPI Interface, active Low Wakeup from SLEEP state I2C: Wakeup from SLEEP state
7	SCK/SCL	Digital Input	SCK: Clock Input for SPI Interface SCL: Clock Input for I2C Interface
8	SDI/A4	Digital Input	SDI: Data Input for SPI Interface A4: Address bit 4 for I2C Interface
9	SDO/SDA	Digital Output	SDO: Data Output for SPI Interface (tri-state when not active)

Pin(TSSOP16)	Name	Pin Function	Description
			SDA: Data I/O for I2C interface
10	MODE	Digital Input	Mode Selection: VSS: Select SPI Interface VCC: Select I2C Interface
11	VCC	Power	Power Supply (3.3V)
12	VDDO	Power	1.8V power output, connect to capacitor
13	XOUT	Analog Output	Crystal Oscillator Output
14	XIN	Analog Input	Crystal Oscillator Input
15	ANTB	RF	Antenna Interface
16	ANT	RF	Antenna Interface

## 6 Block Diagram



## 7 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage and affect device reliability if exceeded.

Parameter	Symbol	Value	Units
Supply Voltage of VCC	VCC	-0.3 to +3.6	V
Supply Voltage of VDDO	VDDO	-0.3 to +2.5	V
Input Voltage	V <sub>IN</sub>	-0.3 to (VCC+0.3)	V
Output Voltage	V <sub>OUT</sub>	-0.3 to (VCC+0.3)	
Operating Temperature	T <sub>OP</sub>	-40 to +85	°C
Storage Temperature	T <sub>ST</sub>	-40 to +125	°C

**Note:** These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

## 8 Electrical Characteristics

(Conditions: VCC=+3V, VSS=0V, TA=−40°C to +85°C)

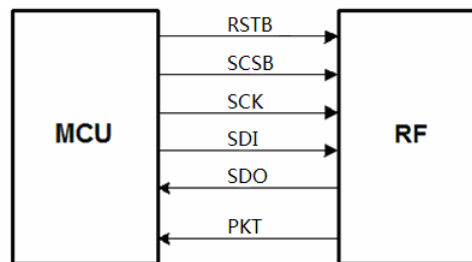
Symbol	Parameter (Condition)	Notes	Min.	Typ.	Max.	Units
<b>Operating Conditions</b>						
VCC	Supply voltage of VCC		1.9	3.3	3.6	V
T <sub>OP</sub>	Operating Temperature		-40		85	°C
<b>Digital Input Pin</b>						
V <sub>IH</sub>	High Level Input Voltage		0.8VCC		1.2VCC	V
V <sub>IL</sub>	Low Level Input Voltage		0		0.2VCC	V
<b>Digital Output Pin</b>						
V <sub>OH</sub>	High Level Output Voltage		0.8VCC		VCC	V
V <sub>OL</sub>	Low Level Output Voltage		0		0.2VCC	V
<b>General RF Conditions</b>						
f <sub>OP</sub>	Operating frequency		2400		2482	MHz
f <sub>XTAL</sub>	Crystal Frequency			12		MHz
Δf <sub>1M</sub>	Frequency Deviation @1Mbps			280		KHz
R <sub>GFSK</sub>	Data Rate			1		Mbps
F <sub>CHANNEL</sub>	Channel Spacing			1		MHz
<b>Transmitter Operation</b>						
P <sub>RF</sub>	Maximum Output Power			0	5.5	dBm
P <sub>RFC</sub>	RF Power Control Range		18	20	22	dB
P <sub>RF1</sub>	1st Adj. Channel TX Power				-20	dBm

Symbol	Parameter (Condition)	Notes	Min.	Typ.	Max.	Units
P <sub>RF2</sub>	2nd Adj. Channel TX Power				-50	dBm
I <sub>VCC_H</sub>	Power Consumption @High Gain			16		mA
I <sub>VCC_L</sub>	Power Consumption @Low Gain			12		mA
<b>Receiver Operation</b>						
I <sub>VCC</sub>	Power Consumption			17		mA
RX <sub>SENS</sub>	RX Sensitivity @0.1%BER			-88		dBm

## 9 SPI Interface

### 9.1 SPI Data and Control

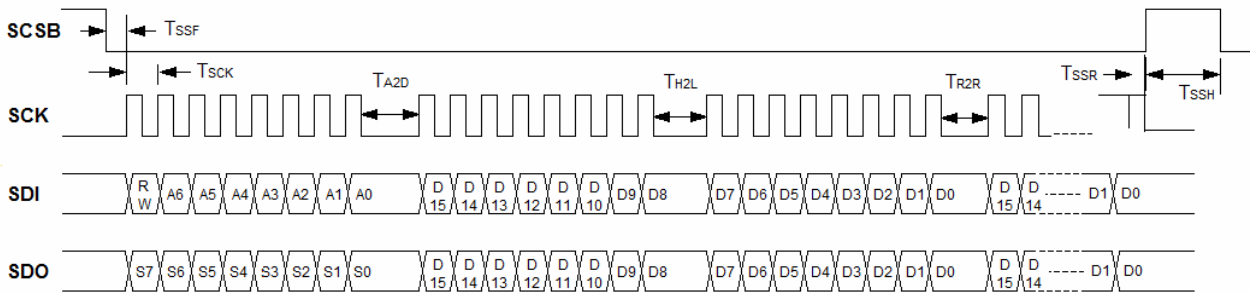
The chip provides a simple interface for application MCU, consisting of SPI interface plus two handshake signals. The chip SPI supports slave mode only.



The data and control interface gives access to all the features in the chip. The data and control interface consists of the following seven digital signals:

Pin	Description
RSTB	Reset Input, active low
MODE	Mode Selection: 0—SPI
SCSB	SPI Slave Select Input Wakeup from SLEEP state
SCK	SPI Clock Input
SDI	SPI Data Input
SDO	SPI Data Output
PKT	Packet TX/RX Flag

## 9.2 SPI Command Format



Name	Min.	Typ.	Max.	Description
$T_{SSH}$	250ns			Interval between two SPI accesses
$T_{SSF}, T_{SSR}$	41.5ns			Relationship between SCSB and SCK
$T_{A2D}$	*1			Interval time between address and data
$T_{H2L}$	*1			Interval time between high byte and low byte data
$T_{R2R}$	*1			Interval time between two register data
$T_{SCK}$	83ns			SCK period

Notes: \*1--When reading FIFO data, at least 450ns wait time is required. Otherwise,  $T_{3min} = 41.5ns$ .

## 10 I2C Interface

### 10.1 I2C Data and Control

Pin	Description
RSTB	Reset Input, active low
MODE	Mode Selection: 1—I2C
SCSB	Wakeup from SLEEP state
SCL	I2C Clock Input
SDA	I2C Data I/O
A4	I2C Address Bit 4

### 10.2 I2C Supported Feature

I2C Slave Mode Optional	Support or Not
Standard-mode – 100 kbps	Yes
Fast-mode – 400 kbps	Yes



I2C Slave Mode Optional	Support or Not
Fast-mode Plus – 1000 kbps	Yes
High-speed mode – 3200 kbps	No
Clock Stretching	No
10-bit slave address	No
general call address	No
software reset	No
device ID	No

### 10.3 I2C Command Format

**Example I2C Data Transfers:**

Master writes 1 or more data bytes to PL1167 FIFO register:



Master writes 1 byte to PL1167 to specify FIFO register, then reads one or more bytes from PL1167 FIFO:



Master may continue reading PL1167 FIFO:



Sr: repeated Start

A: Acknowledge



### 10.4 I2C Device Address

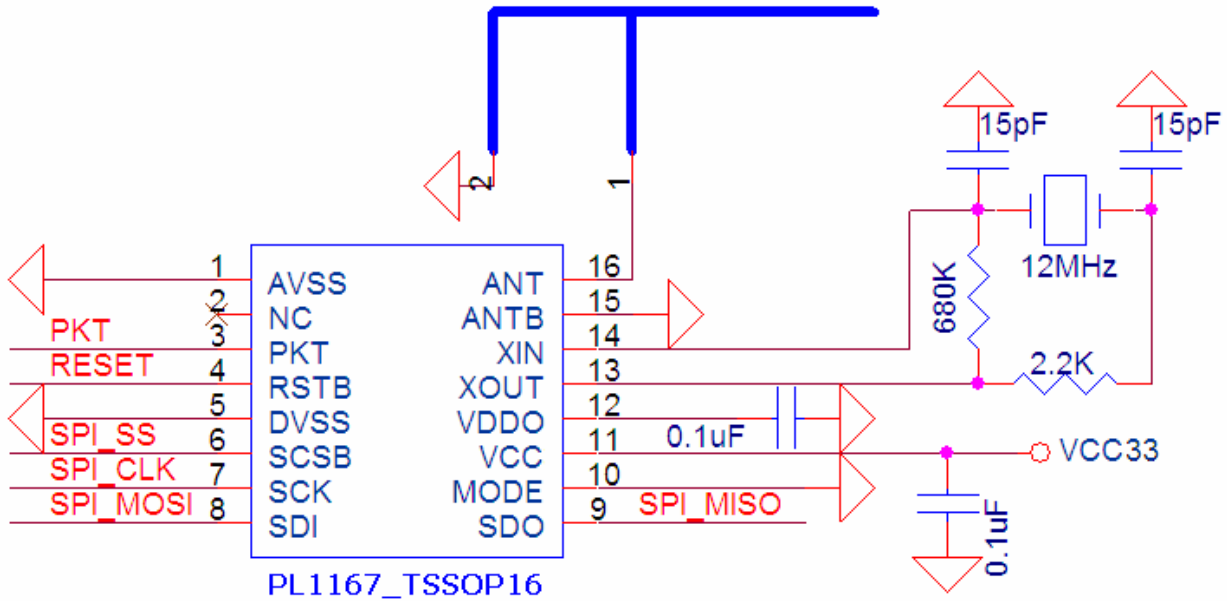
A6	A5	A4	A3	A2	A1	A0	R/W
0	1	A4 Pin	1	0	0	0	Read=1 Write=0

## 11 Control Register Information

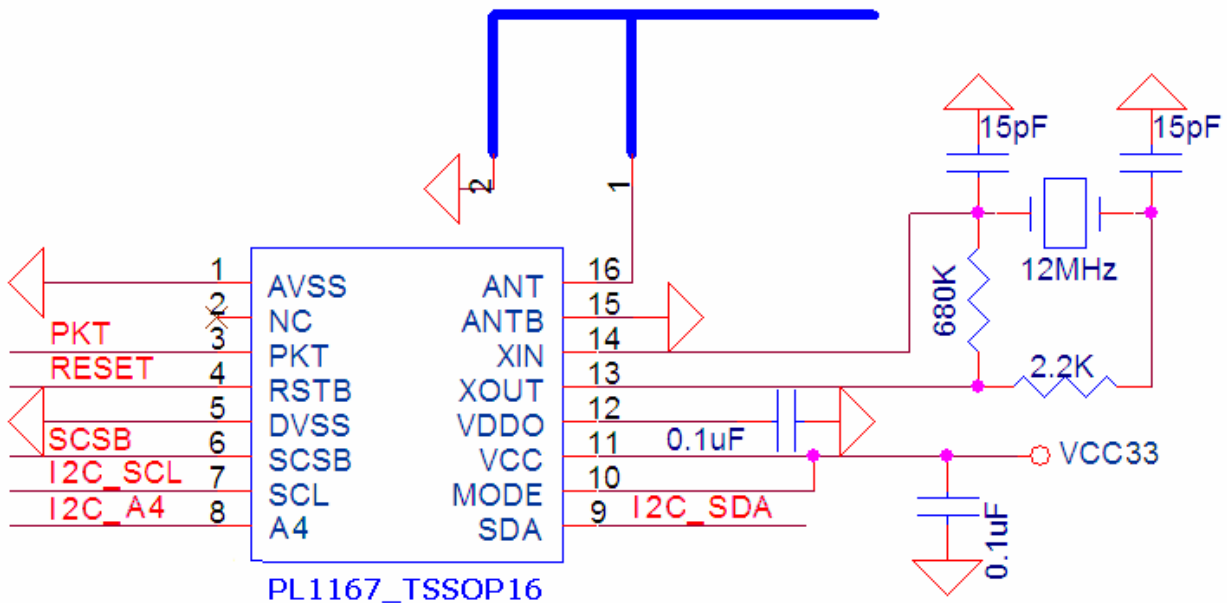
The latest recommended control registers value is in user manual, please contact with POWERLINK.

## 12 Typical Application

### SPI Mode



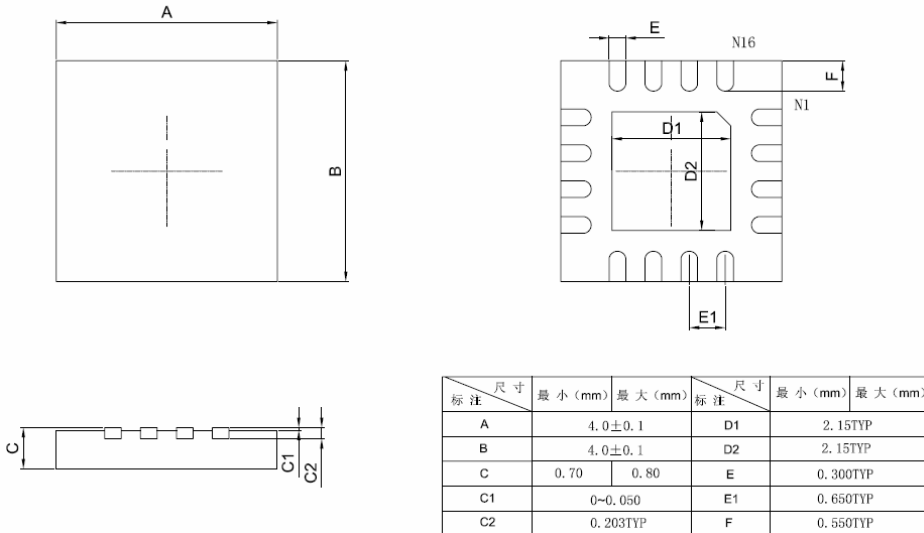
### I2C Mode



# 13 Packaging Information

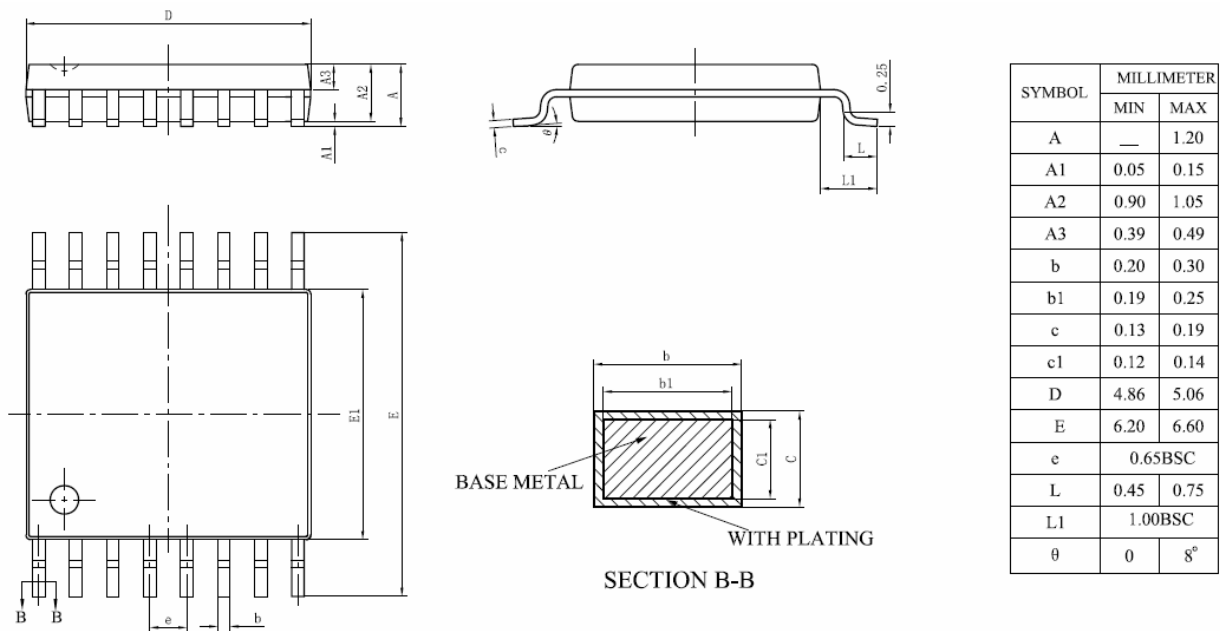
## QFN16 package

QFN16(4x4mm, 0.65mm pitch, Thinner) PACKAGE OUTLINE DIMENSIONS



## TSSOP16 package

TSSOP16 PACKAGE OUTLINE DIMENSIONS



## **14 Important Notice**

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