

PL1167

Low Power High Performance Single Chip 2.4GHz Transceiver

Product Description:

PL1167 is a piece of true low power high performance single chip 2.4GHz transceiver, which is designed for operation in the world wide ISM frequency band at 2.400~2.4835GHz.

This single chip wireless transceiver integrated including: RF synthesizer, Power Amplifier, Crystal Oscillator, Modem and etc.

All of the Output Power, Channel Selection, and Protocol can be configured through SPI Interface.

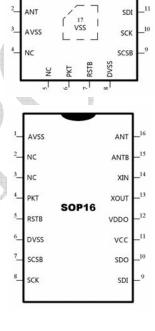
With built in FHSS and accurate digital RSSI, this transceiver achieves a good capability of anti-interference, so that, it can work under every complicated environment with high performance.

It also support address and data check out; FEC, CRC function; and Auto-Ack & Auto-Resend function.

The output power of the chip can be set up to 2dBm and the receive sensitivity can achieve -88dBm.

With on chip regulator and advanced power management function, the current consumption in sleep mode can be reduced to nearly 1uA.

Pin Configuration:



Key Features:

- True Low Power High Performance Single Chip 2.4GHz Transceiver
- Built in Hardware Link Layer
- Built in Accurate Digital RSSI
- Support Auto-Ack and Auto-Resend Functions
- Built in Address and Data Checkout, FEC, CRC Functions
- Data Rate over the air: 1Mbps
- Support SPI Bus Interface
- Support HFSS
- Support Micro-Strip Inductor and Two Layer PCB Boards
- 1.9 to 3.6V supply range
- Packages: QFN16/SOP16

Applications:

- Wireless Mice, keyboards and Game Controllers
- Wireless Data Communication
- Wireless Door Accessing
- Wireless Networks
- Safety and Guard System
- RF Remote Control
- Remote Sensing
- Sports watches and sensors
- Home and commercial automation
- Industrial Sensors
- Industrial and Commercial Short Range Communication
- VoIP headsets
- Toys





1 Overview

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2 Features

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- Built in Hardware Link Layer.
- Built in Accurate Digital RSSI
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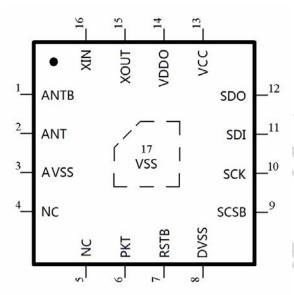
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3 Quick Reference Data

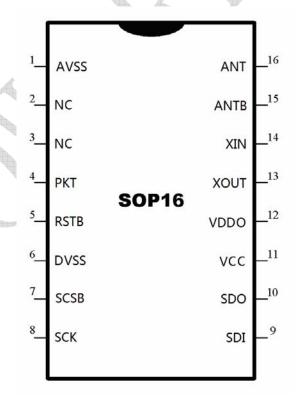
Parameter	Value	Units	
Min Supply Voltage	1.9	V	
Max Output Power	2 dBm		
Data Rate	1	Mbps	
Current Consumption (0dBm) @TX Mode	16	mA	
Current Consumption @RX Mode	17	mA	
Operating Temperature Range	-40 to +85	${\mathbb C}$	
RX Sensitivity	-88	dBm	
Current Consumption @Sleep Mode	1	uA	

4 Pin Diagrams

The pin map is shown as below for QFN16.



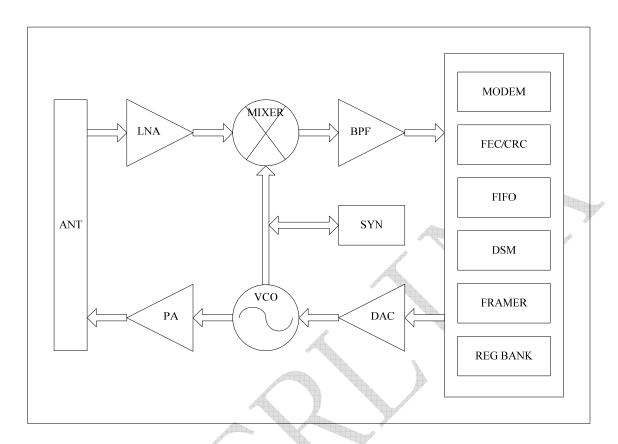
The pin map is shown as below for SOP16.



5 Pin Description

Pin(QFN16)	Name	Pin Function	Description
1	ANTB	RF	Antenna Interface
2	ANT	RF	Antenna Interface
3,8,17	VSS	Power	Ground (0V)
4,5	NC	N/C	Not Connected
6	PKT	Digital Output	Transmit/Receive Packet Status Indicator Bit
7	RSTB	Digital Input	Reset Pin, active low
9	SCSB	Digital Input	Enable Input for SPI Interface, active Low
			Wakeup from SLEEP state
10	SCK	Digital Input	Clock Input for SPI Interface
11	SDI	Digital Input	Data Input for SPI Interface
12	SDO	Digital Output	Data Output for SPI Interface (tri-state when not active)
13	VCC	Power	Power Supply (3.3V)
14	VDDO	Power	1.8V power output, connect to capacitor
15	XOUT	Analog Output	Crystal Oscillator Output
16	XIN	Analog Input	Crystal Oscillator Input

6 Block Diagram



7 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage and affect device reliability if exceeded.

Parameter	Symbol	Value	Units
Supply Voltage of VCC	VCC	-0.3 to +3.6	٧
Supply Voltage of VDDO	VDDO	-0.3 to +2.5	V
Input Voltage	V_{IN}	-0.3 to (VCC+0.3)	V
Output Voltage	V _{OUT}	-0.3 to (VCC+0.3)	
Operating Temperature	T _{OP}	-40 to +85	$^{\circ}$
Storage Temperature	T _{ST}	-40 to +125	$^{\circ}$ C

Note: These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

8 Electrical Characteristics

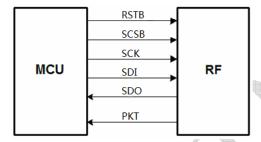
(Conditions: VCC=+3V, VSS=0V, TA= -40° C to +85 $^{\circ}$ C)

Symbol	Parameter (Condition)	Notes	Min.	Тур.	Max.	Units	
	Operating Conditions						
VCC	Supply voltage of VCC		1.9	3.3	3.6	V	
T _{OP}	Operating Temperature		-40		85	$^{\circ}$	
	Digital Input Pin						
V _{IH}	High Level Input Voltage		0.8VCC		1.2VCC	V	
V _{IL}	Low Level Input Voltage		0		0.2VCC	V	
	Digital Output Pin						
V _{OH}	High Level Output Voltage		0.8VCC		VCC	V	
V _{OL}	Low Level Output Voltage		0	The state of the s	0.2VCC	V	
	General RF Conditions						
f _{OP}	Operating frequency		2400	,	2482	MHz	
f _{XTAL}	Crystal Frequency	A		12		MHz	
$\triangle f_{1M}$	Frequency Deviation @1Mbps			280		KHz	
R _{GFSK}	Data Rate			1		Mbps	
F _{CHANNEL}	Channel Spacing			1		MHz	
	Transmitter Operation		>				
P _{RF}	Maximum Output Power			0	2	dBm	
P _{RFC}	RF Power Control Range		18	20	22	dB	
P _{RF1}	1st Adj. Channel TX Power				-20	dBm	
P _{RF2}	2nd Adj. Channel TX Power				-50	dBm	
I _{VCC_H}	Power Consumption @High Gain			16		mA	
I _{VCC_L}	Power Consumption @Low Gain			12		mA	
	Receiver Operation						
I _{VCC}	Power Consumption			17		mA	
RX _{SENS}	RX Sensitivity @0.1%BER	-		-88		dBm	

9 SPI Interface

9.1 SPI Data and Control

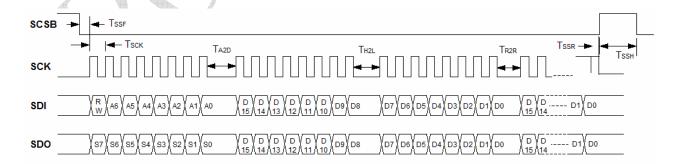
The chip provides a simple interface for application MCU, consisting of SPI interface plus two handshake signals. The chip SPI supports slave mode only.



The data and control interface gives access to all the features in the chip. The data and control interface consists of the following seven digital signals:

Pin	Description		
RSTB	Reset Input, active low		
SCSB	SPI Slave Select Input		
/	Wakeup from SLEEP state		
SCK	SPI Clock Input		
SDI	SPI Data Input		
SDO	SPI Data Output		
PKT	Packet TX/RX Flag		

9.2 SPI Command Format



Name	Min.	Тур.	Max.	Description
T _{SSH}	250ns			Interval between two SPI accesses
T_{SSF},T_{SSR}	41.5ns			Relationship between SCSB and SCK

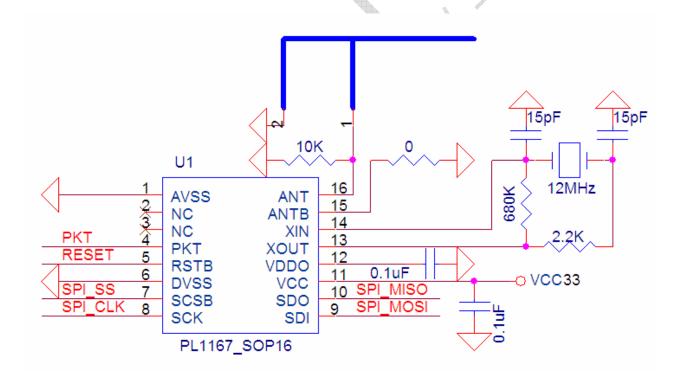
Name	Min.	Тур.	Max.	Description
$T_{\mathtt{A2D}}$	*1			Interval time between address and data
T _{H2L}	*1			Interval time between high byte and low byte data
$T_{\mathtt{R2R}}$	*1			Interval time between two register data
T _{SCK}	83ns			SCK period

Notes: *1--When reading FIFO data, at least 450ns wait time is required. Otherwise, $T3_{min} = 41.5$ ns.

10 Control Register Information

The latest recommended control registers value is in user manual, please contact with POWERLINK.

11 Typical Application



2. 15TYP

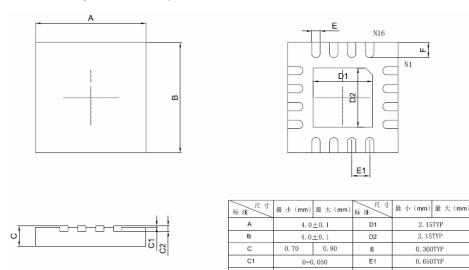
0. 300TYP

0. 650TYP

12 Packaging Information

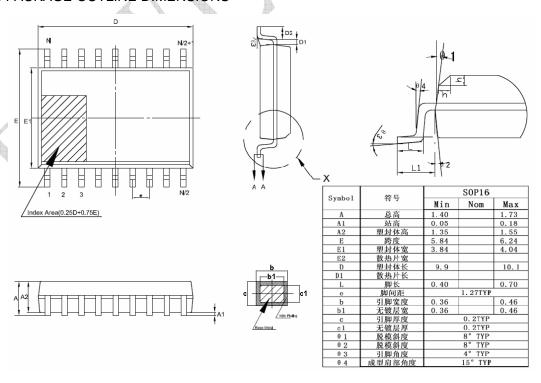
QFN16 package

QFN16(4x4mm, 0.65mm pitch, Thinner) PACKAGE OUTLINE DIMENSIONS



SOP16 package

SOP16 PACKAGE OUTLINE DIMENSIONS



13 Important Notice

POWERLINK reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

